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# FIBOCOM NL668-EU Series

## Hardware User Manual

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## Applicability type

No.	Product model	Description
1	NL668-EU-01	MCP is 4+2, supports MAIN_ANT, DIV_ANT, GNSS_ANT
2	NL668-EU-00	Based on NL668-EU-01,don't support TDD
3	NL668-EU-03	Based on NL668-EU-01,change MCP to 2+1, update function definition of some pins

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## Versions Record

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V1.0.1	Zhengyang Gaotianhuan Heruzhi	Tumin/Lixiyi	Tumin Lixiyi	2019-05-05	1. Updata RF parameters, standardize document formats 2. Add NL668-EU-03 product description

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# 1 Introduction

## 1.1 Document Introduction

This document describes the electrical characteristics, RF performance, structure size, application environment, etc. of NL668-EU module. With the assistance of the document and other instructions, the developers can quickly understand the hardware functions of the NL668-EU module and develop products.

## 1.2 Safety precautions

By following the safety guidelines below, you can protect the personal safety and help protect the product and work environment from potential damage. Product manufacturers need to communicate the following safety instructions to end users. In case of failure to comply with these safety rules, Fibocom will not be responsible for the consequences caused by the user's misuse.



Road safety first! When you drive, do not use the handheld devices even if it has a hand-free feature. Please stop and call!



Please turn off the mobile device before boarding. The wireless feature of the mobile device is not allowed on the aircraft to prevent interference with the aircraft communication system. Ignoring this note may result in flight safety issue or even breaking the law.



When in a hospital or health care facility, please be aware of restrictions on the use of mobile devices. Radio frequency interference may cause medical equipment to malfunction, so it may be necessary to turn off the mobile device.



The mobile device does not guarantee that an effective connection can be made under any circumstances, for example, when there is no prepayment for the mobile device or the (U)SIM is invalid. When you encounter the above situation in an emergency, remember to use an emergency call, while keeping your device turned on and in areas where signal is strong.



Your mobile device receives and transmits RF signals when it is powered on. Radio interference occurs when it is near televisions, radios, computers, or other electronic devices.



Keep the mobile device away from flammable gases. Turn off the mobile device when near gas stations, oil depots, chemical plants or explosive workplaces. There is a safety hazard in operating electronic equipment in any potentially explosive environment.

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## 2 Product Overview

### 2.1 Product Introduction

The NL668-EU series wireless module is a broadband wireless terminal product applicable to various network formats and multi-bands include TDD-LTE/FDD-LTE/WCDMA/GSM.

### 2.2 Product Specification

Specification		
Operating frequency	NL668-EU-01/03	LTE FDD: Band 1,3,5,7,8,20
		LTE TDD: Band 38,40,41
		WCDMA: Band 1,5,8
		GSM/GPRS/EDGE: 850/900/1800MHz
	NL668-EU-00	LTE FDD: Band 1,3,5,7,8,20
		WCDMA: Band 1,5,8
		GSM/GPRS/EDGE: 850/900/1800MHz
Data transmission	LTE FDD Rel.9	150Mbps DL/50Mbps UL(Cat 4); LTE Downlink MIMO 2x2, 4x2 (support part of R10)
	LTE TDD Rel.9	130Mbps DL/30.5MbpsUL(Cat 4); LTE Downlink MIMO 2x2, 4x2 (support part of R10)
	WCDMA Rel.8	WCDMA:384 kbps DL/384 kbps UL
		DC-HSDPA+:42Mbps (Cat 24)/HSUPA:5.76Mbps (Cat 6)
	GPRS/EDGE Rel.5	GPRS: 107kbps/85.6kbps UL (multi-slot class 33)
		EDGE(E-GPRS):296kbps DL/236.8kbps UL (multi-slot class 33)
Power	3.3V~4.3V (3.8V recommended)	
Temperature	Normal: -30°C~+75°C	
	Extended: -40°C~+85°C	
	Storage: -40°C~+85°C	
Power consumption	Base current: <2mA	
	Sleep mode: ≤3mA(USB sleep)	

	Idle mode: <20mA (USB sleep) ;<29mA (USB wake up)
Physical characteristics	Package: LCC+LGA 144PIN
	Size: 32.0×29.0×2.4 mm
	Weight: About 5.5g
<b>Interface</b>	
Antenna	Antenna: Main x 1, GNSS x 1, DIV x 1
Functional Interface	(U)SIM 3.0V/1.8V
	USB 2.0 x 1
	UART x 2, PCM, I2C, SGMII, SDIO, GPIO, SPI, WAKEUP_IN
	Status Indicator
	ADC x 2
<b>Software</b>	
Protocol Stack	Embedded TCP/IP and UDP/IP protocol stack
AT Command	3GPP TS 27.007 and 27.005, and proprietary FIBOCOM AT
Firmware update	USB (UART does not support DOWNLOAD)
Voice service	VoLTE, HR, FR, EFR, AMR, DTMF, Caller ID, Call Transfer, Call Hold, Call Waiting and Multi-Talk, etc.
SMS	point-to-point MO, MT; cell broadcast; support Text and PDU modes
MMS service	Need AP to realize MMS protocol

Table 2-1 Product Specification



**Note:**

When the temperature is beyond the normal operating temperature range (-30 °C to + 75 °C), the RF performance of the module may slightly exceed the 3GPP specification.

## 2.3 Functional Diagram

Functional diagram shows the main hardware features of the NL668-EU series module, including baseband and RF features.

Baseband includes:

- PMIC
- MCP
- USB, (U)SIM, PCM, I<sup>2</sup>C, SPI, UART, SGMII, SDIO, GPIOs

RF includes:

- RF Transceiver
- RF PA
- RF filter
- Antenna

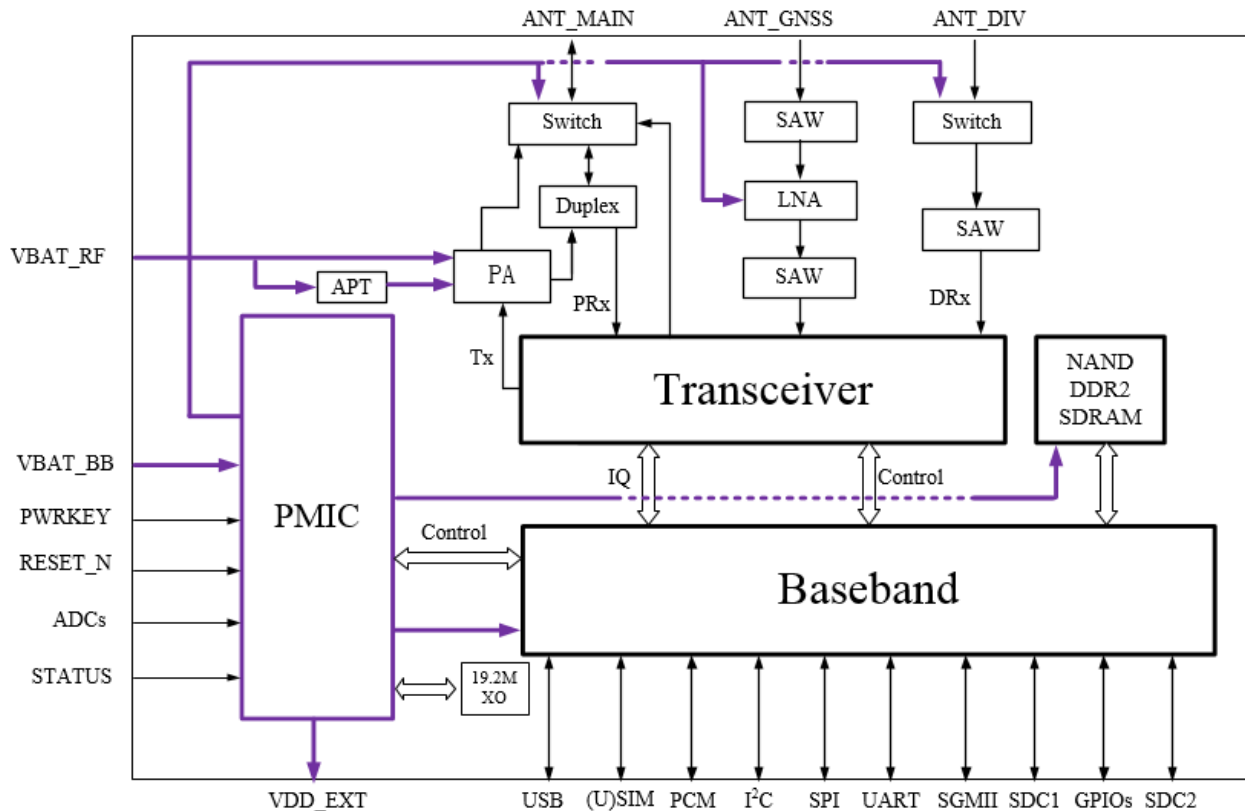


Figure 2-1 Functional Diagram

## 2.4 Evaluation Board

Fibocom provide EVK-GT8230-NL, ADP-NL668-CN-00-00, ADP-NL668-LA-00-00 evaluation board to convenient module's debug and use.

## 3 Pin Description

### 3.1 Pin Assignment

The NL668-EU series module is available in 144 pins. The numbers of the LCC pins are 80, and the LGA pins are 64. the top view of the pin assignment is shown as follow figure:

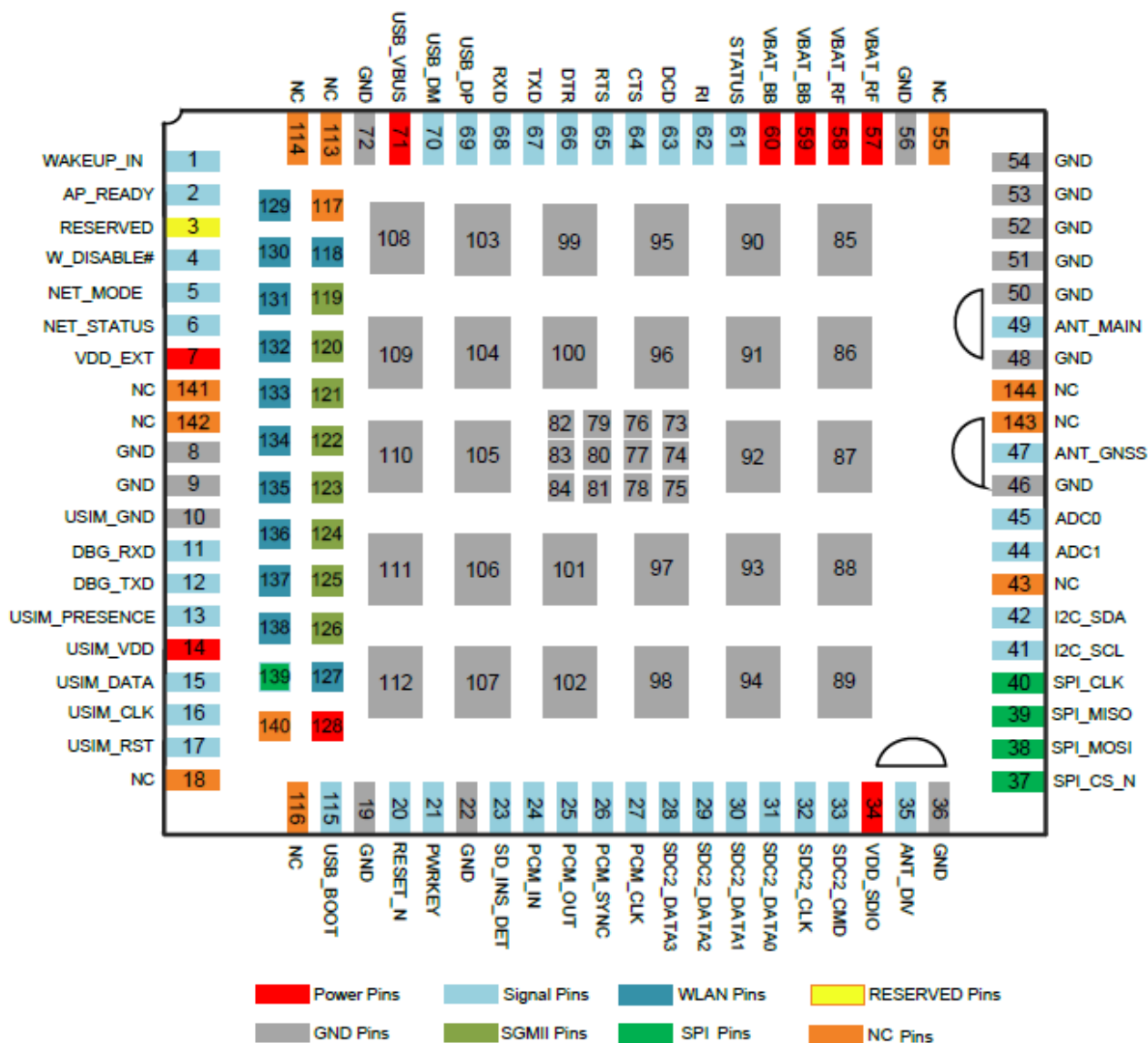


Figure 3-1 Pin Assignment (Top View Diagram)



Note: Pin 73~112 of NL668-EU-00/01 is the thermal pins, and the module is grounded internally. It is recommended that the heat sink pad is reserved for PCB packaging and welded.

Pin 74~75 and 77~84 of NL668-EU-03 is not ground , please reference the pin function description of NL668-EU-03.

## 3.2 Pin function

The pin function description of NL668-EU series module is shown as table 3-1:

Pin Num	Pin Name	I/O	Level	Description
1	WAKEUP_IN	I	V <sub>ILmin</sub> =-0.3V V <sub>ILmax</sub> =0.6V V <sub>IHmin</sub> =1.2V V <sub>IHmax</sub> =2.0V	External device wake-up module, low level active by default with software programmable option
2	AP_READY	I	V <sub>ILmin</sub> =-0.3V V <sub>ILmax</sub> =0.6V V <sub>IHmin</sub> =1.2V V <sub>IHmax</sub> =2.0V	Reserved
3	RESERVED	-	-	Reserved
4	W_DISABLE#	I	V <sub>ILmin</sub> =-0.3V V <sub>ILmax</sub> =0.6V V <sub>IHmin</sub> =1.2V V <sub>IHmax</sub> =2.0V	Module airplane mode control. Pull up by default, pull down this pin, module enter airplane mode
5	NET_MODE	O	V <sub>OLmax</sub> =0.45V V <sub>OHmin</sub> =1.35V	Module network state indicate(by default)
6	NET_STATUS	O	V <sub>OLmax</sub> =0.45V V <sub>OHmin</sub> =1.35V	Module network state indicate
7	VDD_EXT	PO	1.8V	Module digital level, 1.8V output, 80mA
8	GND	G	-	Ground
9	GND	G	-	Ground
10	GND	G	-	Ground
11	DBG_RXD	I	V <sub>ILmin</sub> =-0.3V V <sub>ILmax</sub> =0.6V V <sub>IHmin</sub> =1.2V V <sub>IHmax</sub> =2.0V	Receive data
12	DBG_TXD	O	V <sub>OLmax</sub> =0.45V V <sub>OHmin</sub> =1.35V	Transmit data
13	USIM_PRESENCE	I	V <sub>ILmin</sub> =-0.3V V <sub>ILmax</sub> =0.6V V <sub>IHmin</sub> =1.2V V <sub>IHmax</sub> =2.0V	(U)SIM card hot plug detection
14	USIM_VDD	PO	For 1.8V (U)SIM: V <sub>max</sub> =1.9V	(U)SIM power. Module identify 1.8V and 3V (U)SIM card automatically. Dual voltage (1.8/2.85 V)



Pin Num	Pin Name	I/O	Level	Description
			V <sub>min</sub> =1.7V For 3.0V (U)SIM: V <sub>max</sub> =3.05V V <sub>min</sub> =2.7V I <sub>omax</sub> =50mA	
15	USIM_DATA	IO	For 1.8V (U)SIM: V <sub>ILmax</sub> =0.6V V <sub>IHmin</sub> =1.2V V <sub>OLmax</sub> =0.45V V <sub>OHmin</sub> =1.35V For 3.0V (U)SIM: V <sub>ILmax</sub> =1.0V V <sub>IHmin</sub> =1.95V V <sub>OLmax</sub> =0.45V V <sub>OHmin</sub> =2.55V	(U)SIM data signal
16	USIM_CLK	O	For 1.8V (U)SIM: V <sub>OLmax</sub> =0.45V V <sub>OHmin</sub> =1.35V For 3.0V (U)SIM: V <sub>OLmax</sub> =0.45V V <sub>OHmin</sub> =2.55V	(U)SIM clock signal
17	USIM_RST	O	For 1.8V (U)SIM: V <sub>OLmax</sub> =0.45V V <sub>OHmin</sub> =1.35V For 3.0V (U)SIM: V <sub>OLmax</sub> =0.45V V <sub>OHmin</sub> =2.55V	(U)SIM reset signal
18	NC	-	-	NC
19	GND	G	-	Ground
20	RESET_N	I	V <sub>IHmax</sub> =2.1V	Module reset signal, active low, pull up

Pin Num	Pin Name	I/O	Level	Description
			$V_{IHmin}=1.3V$ $V_{ILmax}=0.5V$	1.8V internally, no need pull up externally
21	PWRKEY	I	$V_{IHmax}=2.1V$ $V_{IHmin}=1.3V$ $V_{ILmax}=0.5V$	Module turn on/off signal, active low, no need pull up externally. Because the input is pulled up to an internal voltage minus a diode drop. As per the design, this causes the voltage of the pin is 0.8V after power the module.
22	GND	G	-	Ground
23	SD_INS_DET	I	-	Reserved
24	PCM_IN	I	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	PCM input signal
25	PCM_OUT	O	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	PCM output signal
26	PCM_SYNC	IO	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$ $V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	PCM synchronization signal
27	PCM_CLK	IO	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$ $V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	PCM clock signal
28	SDC2_DATA3	IO	-	Reserved
29	SDC2_DATA2	IO	-	Reserved
30	SDC2_DATA1	IO	-	Reserved
31	SDC2_DATA0	IO	-	Reserved
32	SDC2_CLK	O	-	Reserved
33	SDC2_CMD	IO	-	Reserved
34	VREG_L13_2P85	PO	-	Reserved
35	ANT_DIV	I	-	Diversity antenna
36	GND	G	-	Ground

Pin Num	Pin Name	I/O	Level	Description
37	SPI_CS_N	O	-	Reserved
38	SPI_MOSI	O	-	Reserved
39	SPI_MISO	I	-	Reserved
40	SPI_CLK	O	-	Reserved
41	I2C_SCL	OD	-	I2C interface clock signal
42	I2C_SDA	OD	-	I2C interface data signal
43	NC	-	-	NC
44	ADC1	I	-	Analog to digital converter interface 1
45	ADC0	I	-	Analog to digital converter interface 0
46	GND	G	-	Ground
47	ANT_GNSS	I	-	GNSS antenna
48	GND	G	-	Ground
49	ANT_MAIN	IO	-	Main antenna
50	GND	G	-	Ground
51	GND	G	-	Ground
52	GND	G	-	Ground
53	GND	G	-	Ground
54	GND	G	-	Ground
55	NC	-	-	NC
56	GND	G	-	Ground
57	VBAT_RF	I	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	RF power input (3.3V~4.3V)
58	VBAT_RF	I	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	RF power input (3.3V~4.3V)
59	VBAT_BB	I	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	Baseband power input (3.3V~4.3V)
60	VBAT_BB	I	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	Baseband Power Input (3.3V~4.3V)
61	STATUS	O	VOLmax=0.45V VOHmin=1.35V	Module network state indicate
62	RI	O	VOLmax=0.45V	Module output ring indicator

Pin Num	Pin Name	I/O	Level	Description
			$V_{OHmin}=1.35V$	
63	DCD	O	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	Module output data carrier detection
64	CTS	I	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	Clear to send ( apply to NL668-EU-00/01 )
		O	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	Send data requirement ( apply to NL668-EU-03 )
65	RTS	O	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	Send data requirement ( apply to NL668-EU-00/01 )
		I	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	Clear to send t( apply to NL668-EU-03 )
66	DTR	I	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	Data ready. The control of module sleep mode
67	TXD	O	$V_{OLmax}=0.45V$ $V_{OHmin}=1.35V$	Transmit data
68	RXD	I	$V_{ILmin}=-0.3V$ $V_{ILmax}=0.6V$ $V_{IHmin}=1.2V$ $V_{IHmax}=2.0V$	Receive data
69	USB_DP	IO	Conform to USB2.0 standard specification	USB differential data bus (+)
70	USB_DM	IO	Conform to USB2.0 standard specification	USB differential data bus (-)
71	USB_VBUS	PI	$V_{max}=5.25V$	USB plug detection

Pin Num	Pin Name	I/O	Level	Description
			Vmin=3.0V Vnorm=5.0V	
72	GND	G	-	Ground
73	GND	G		Ground(apply to NL668-EU-00/01)
	WDOG_DISABLE	I/O		Reserved(apply to NL668-EU-03)
74~75, 77~84	GND	G		Ground(apply to NL668-EU-00/01)
	NC	-		NC(apply to NL668-EU-03)
76,85~112	GND	G		Ground
113	NC	-	-	NC
114	NC	-	-	NC
115	USB_BOOT	I	V <sub>IL</sub> min=-0.3V V <sub>IL</sub> max=0.6V V <sub>IH</sub> min=1.2V V <sub>IH</sub> max=2.0V	Emergency download, active high, recommended to reserve test point
116	NC	-	-	NC
117	NC	-	-	NC(apply to NL668-EU-00/01)
	RF_CLK	O	-	Reserved(apply to NL668-EU-03)
118	WLAN_SLP_CLK	O	-	Reserved
119	EPHY_RST_N	O	-	Reserved
120	EPHY_INT_N	I	-	Reserved
121	SGMII_MDATA	IO	-	Reserved
122	SGMII_MCLK	O	-	Reserved
123	SGMII_TX_M	O	-	Reserved
124	SGMII_TX_P	O	-	Reserved
125	SGMII_RX_P	I	-	Reserved
126	SGMII_RX_M	I	-	Reserved
127	PM_ENABLE	O	--	Reserved
128	VREG_L5_UIM2	PO	-	Reserved
129	SDC1_DATA3	IO	-	Reserved
130	SDC1_DATA2	IO	-	Reserved
131	SDC1_DATA1	IO	-	Reserved
132	SDC1_DATA0	IO	-	Reserved
133	SDC1_CLK	O		Reserved
134	SDC1_CMD	O	-	Reserved
135	WAKE_WLAN	I		Reserved

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Pin Num	Pin Name	I/O	Level	Description
136	WLAN_EN	O	-	Reserved
137	COEX_UART_RXD	I	-	Reserved
138	COEX_UART_TXD	IO	-	Reserved
139	BT_EN	O	-	Reserved
140	NC	-	-	NC
141	NC	-	-	NC(apply to NL668-EU-00/01)
	I2C_SCL	IO		Reserved(apply to NL668-EU-03)
142	NC	-	-	NC(apply to NL668-EU-00/01)
	I2C_SDA	IO		Reserved(apply to NL668-EU-03)
143	NC	-	-	NC(apply to NL668-EU-00/01)
	GRFC1	O		Reserved(apply to NL668-EU-03)
144	NC	-	-	NC(apply to NL668-EU-00/01)
	GRFC0	O		Reserved(apply to NL668-EU-03)

Table 3-1 Pin function description



**Note:**

Keep the unused pins floating.

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## 4 Electrical characteristics

### 4.1 Power

Table 4-1 show the power interface of NL668-EU series module.

Pin Name	I/O	Pin	Description
VBAT_RF	I	57,58	Module power supply, 3.3V~4.3V, typical value 3.8V
VBAT_BB	I	59,60	Module power supply, 3.3V~4.3V, typical value 3.8V
VDD_EXT	O	7	Module digital voltage output, 1.8V, 80mA
GND	-	8,9,10,19,22,36,46,48,5 0~54,56,72~112	All GND pins must be grounded(apply to NL668-EU-00/01)
		8,9,10,19,22,36,46,48,5 0~54,56,72,76,85~112	GND(apply to NL668-EU-03)

Table 4-1 Power Interface



**Note:**

In the rest of the document, VBAT includes VBAT\_BB and VBAT\_RF.

### 4.2 Power supply

The NL668-EU series module needs to be powered by the VBAT pin. The recommend power design is shown in Figure 4-1:

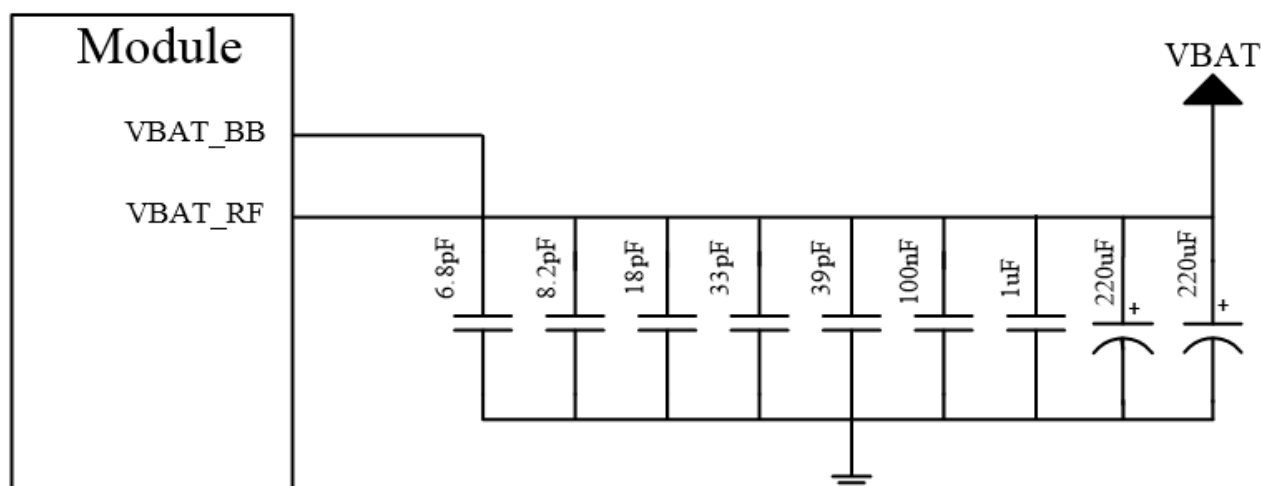


Figure 4-1 Recommend Power Design

Table 4-1 is the filter capacitors design of power supply:

Recommended capacitor	Application	Description
220uF x 2	Regulating capacitor	Reduce power fluctuations during module operation, requiring low ESR Capacitor LDO or DCDC power requires not less than 440uF capacitor Battery power can be properly reduced to 100uF ~ 220uF capacitor
1uF, 100nF	Digital signal noise	Filter clock and digital signal interference
39pF, 33pF	700, 850/900 MHz bands	Filter low band RF interference
18pF, 8.2pF, 6.8pF	1700/1800/1900, 2100/2300, 2500/2600MHz bands	Filter middle/high band RF interference

Table 4-2 Filter Capacitors Design of Power Supply

The power stability can ensure the normal operation of NL668-EU module. The power supply ripple limit for the module is no more than 300mV (the circuit ESR < 100mΩ) requires special attention when design circuit. When the module is operating in GSM mode (Burst transmit), the maximum operating current can reach 3A, and the power voltage needs to be at least 3.3V. Otherwise, the module may power off or restart. The power limit is shown in Figure 4-2:

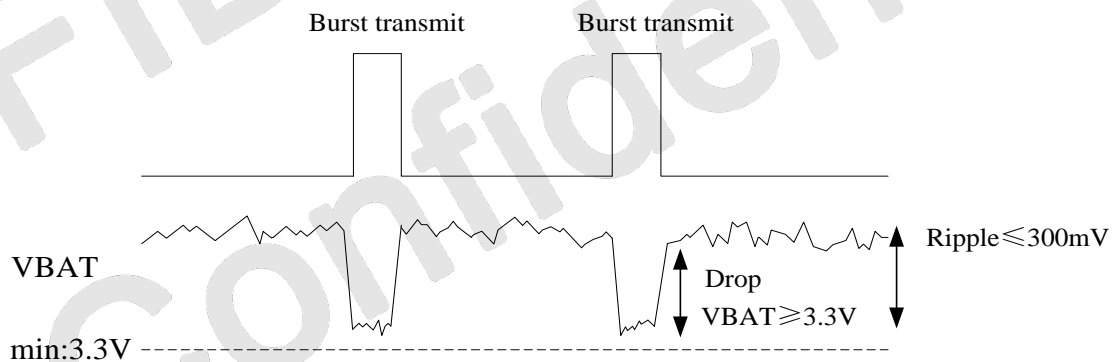


Figure 4-2 Power Limit

## 4.3 1.8V output

The NL668-EU series module outputs a 1.8V voltage through the VDD\_EXT for the use of the internal digital circuit of module. The voltage is the logic level of the module and can be used to indicate module Power on/off, or for external low current (<80mA) circuits. leave the signal floating if no use. The logic level of VDD\_EXT is defined as follows:



Parameter	Minimum	Typical	Maximum	Unit
VDD_EXT	1.71	1.8	1.89	V

Table 4-3 VDD\_EXT Logic Level

## 4.4 Power consumption

The power consumption of NL668-EU module in the case of 3.8V power supply is shown in the following table. (when test please use AT command( at+syscmd=start\_pcm stop ) to close codec function)

Parameter	Mode	Condition	Average Current Typ. (mA)
$I_{off}$	Power off	Power supply, module power off	0.018
$I_{Sleep}$	GSM	MFRMS 2(USB Sleep)	$\leq 2.6$
		MFRMS 5(USB Sleep)	$\leq 2.6$
		MFRMS 9(USB Sleep)	$\leq 2.6$
	WCDMA	DRX=6(USB Sleep)	$\leq 3$
		DRX=7(USB Sleep)	$\leq 3$
		DRX=8(USB Sleep)	$\leq 3$
		DRX=9(USB Sleep)	$\leq 3$
	LTE FDD	Paging cycle #64 frames(USB Sleep)	$\leq 3$
		Paging cycle #128 frames(USB Sleep)	$\leq 3$
		Paging cycle #256 frames(USB Sleep)	$\leq 3$
	LTE TDD	Paging cycle #64 frames(USB Sleep)	$\leq 3$
		Paging cycle #128 frames(USB Sleep)	$\leq 3$
		Paging cycle #256 frames(USB Sleep)	$\leq 3$
$I_{Idle}$	GSM	MFRMS=5( USB sleep)	$\leq 15$
		MFRMS=5 USB (wake up)	$\leq 29$
	WCDMA	DRX=8 Paging cycle #256 frames( USB sleep)	$\leq 15$
		DRX=8 Paging cycle #256 frames (USB wake up)	$\leq 29$
	LTE FDD	DRX=8 Paging cycle #256 frames( USB sleep)	$\leq 15$
		DRX=8 Paging cycle #256 frames (USB wake up)	$\leq 29$
	LTE TDD	DRX=8 Paging cycle #256 frames (USB sleep)	$\leq 15$
		DRX=8 Paging cycle #256 frames( USB wake up)	$\leq 29$
Radio off	Flight	AT+CFUN=0 (USB sleep)	$\leq 10$

Parameter	Mode	Condition	Average Current Typ. (mA)
	mode		
	Flight mode	AT+CFUN=0 (USB wake up)	≤25
I <sub>GSM-RMS</sub>	GSM	EGSM900 PCL5	≤260
		DCS1800 PCL0	≤180
		GSM850 PCL5	≤260
I <sub>GPRS-RMS</sub> CS4	GPRS	GPRS Data transfer GSM900; PCL=5; 1Rx/4Tx	≤500
		GPRS Data transfer GSM8500; PCL=5; 1Rx/4Tx	≤565
		GPRS Data transfer DCS1800; PCL=0; 1Rx/4Tx	≤520
I <sub>EGPRS-RMS</sub> MCS9	EDGE	EDGE Data transfer GSM900; PCL=8; 1Rx/4Tx	≤500
		EDGE Data transfer GSM850; PCL=8; 1Rx/4Tx	≤500
		EDGE Data transfer DCS1800; PCL=2; 1Rx/4Tx	≤450
I <sub>WCDMA-RMS</sub>	WCDMA	WCDMA Data transfer Band I @+23.5dBm	≤780
		WCDMA Data transfer Band V @+23.5dBm	≤700
		WCDMA Data transfer Band VIII @+23.5dBm	≤600
I <sub>LTE-RMS</sub>	LTE FDD	LTE FDD Data transfer Band 1 @+23dBm	≤780
		LTE FDD Data transfer Band 3 @+23dBm	≤790
		LTE FDD Data transfer Band 5 @+23dBm	≤700
		LTE FDD Data transfer Band 7 @+23dBm	≤790
		LTE FDD Data transfer Band 8 @+23dBm	≤620
		LTE FDD Data transfer Band 20 @+23dBm	≤700
	LTE TDD	LTE TDD Data transfer Band 38 @+23dBm	≤430
		LTE TDD Data transfer Band 40 @+23dBm	≤440
		LTE TDD Data transfer Band 41 @+23dBm	≤430



Table 4-4 Power Consumption

**Note :**

USB sleep should send AT command at+gtusbsleepen=2,0

## 5 Functional interface

### 5.1 Control interface

Control interfaces used for module power on/off, and reset operations. The pin definitions are as follows:

Pin name	I/O	Pin Num.	Description
RESET_N	I	20	When the module in operating mode, pull down RESET_N 700ms~1s, and then release it, module WI reset
PWRKEY	I	21	When module in power off mode, pull down PWRKEY 100ms~2s, and then release it, the module will power on; When module in operating mode, pull down PWRKEY 3s~8s, and then release it, the module will power off

Table 5-1 Control Signal

#### 5.1.1 Power on/off

##### 5.1.1.1 Power on

When NL668-EU series module in power off mode, pull down PWRKEY pin 100ms~2s, the module will power on, it is recommended to use OC/OD drive circuit to control PWRKEY pin. The OC drive reference circuit is shown as follows:

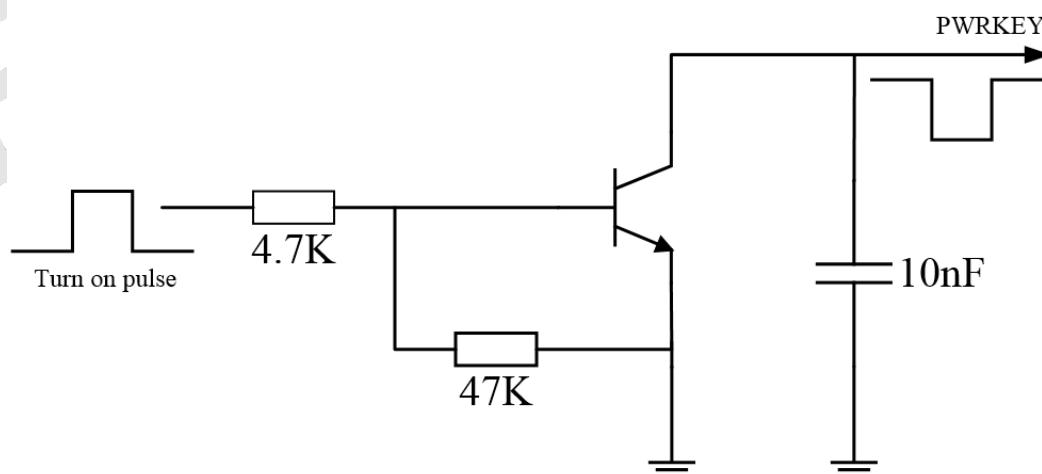


Figure 5-1 OC Drive Power on Reference Circuit

The other way to control PWRKEY pin is use a button switch, a TVS Located near the button (recommended ESD9X5VL-2/TR) for ESD protection. The button switch power on reference circuit is shown as follows:

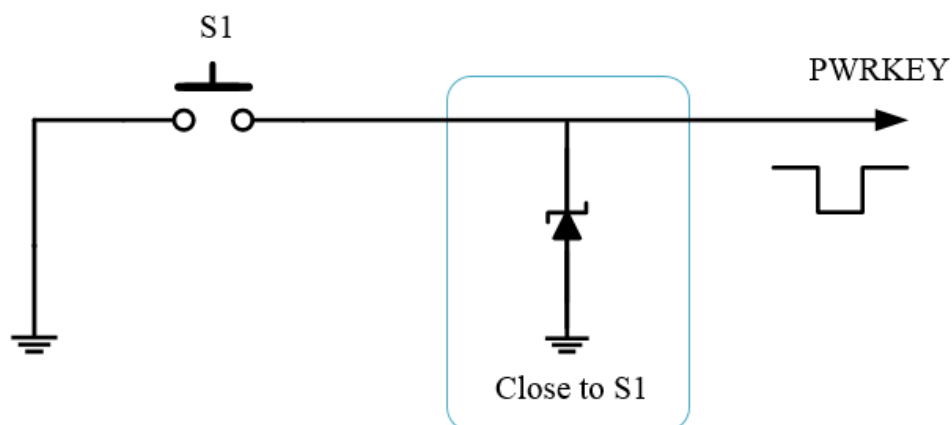


Figure 5-2 Button Switch Power on Reference Circuit

Figure 5-3 is power on timing.

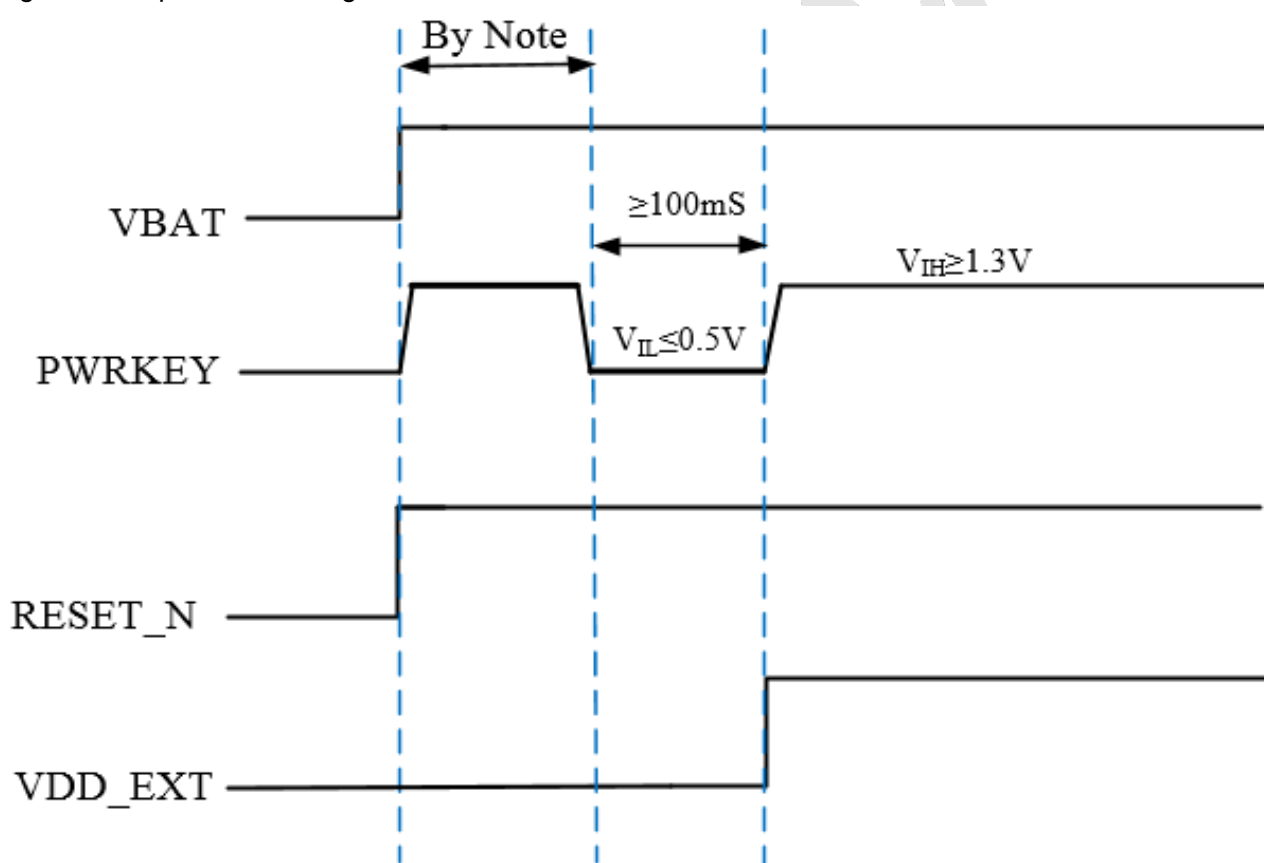


Figure 5-3 Power on Timing



**Note:**

Before pull down PWRKEY pin, the Voltage of VBAT must be stable, recommended time interval between VBAT enable and pull down PWRKEY pin at least 30ms.

## 5.1.1.2 Power off

The module supports three power off methods as table 5-2.

Power off mode	Power off methods	Applicable scenarios
Low-voltage power off	When VBAT voltage is low or power down, the module will power off	The module does not power off through normal process, i.e. does not logout from the base station
Hardware power off	Pull down PWRKEY 3s~8s	Hardware normal power off
AT power off	AT+ CPWROFF	Software normal power off

Table 5-2 Power off



**Note:**

1. When module in operating modes, please do not cut off module power supply to avoid damage internal Flash. Recommended by PWRKEY pin or AT commands power off module, then cut off power supply.

2. When Power off by AT commands, please don't pull down PWRKEY pin, otherwise module will power on again automatically.

The power off timing is shown as follows:

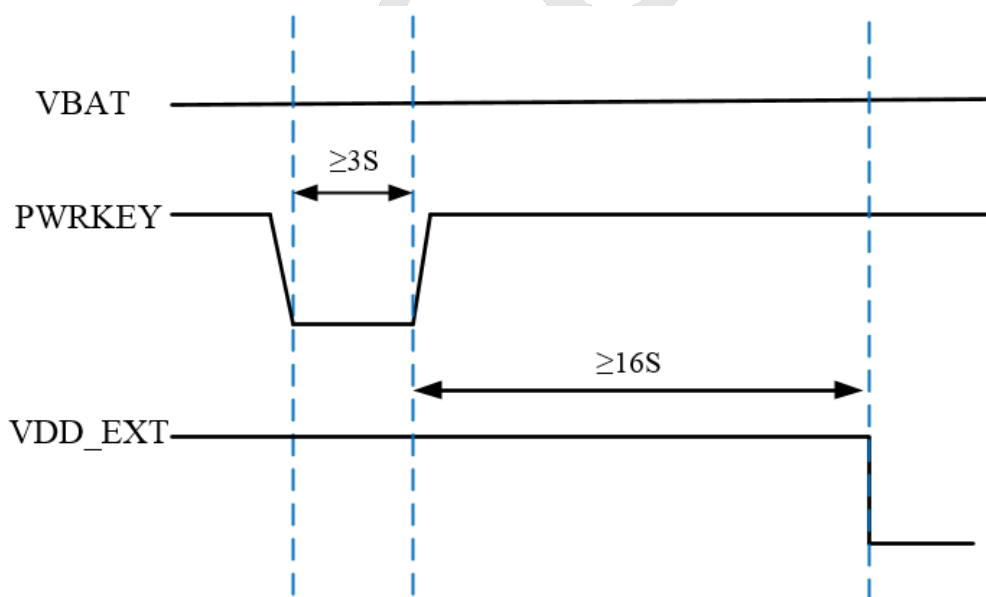


Figure 5-4 Power off Timing

## 5.1.2 RESET

The module supports two mode to reset: hardware reset and software reset.

Reset mode	Reset method
Hardware reset	Pull down RESET_N pin 700s~1s, then release it
Software reset	Sent AT commands AT+RESET

Table 5-3 Module Reset

Clients can control RESET\_N pin by two modes: OC/OD drive circuits and button switch, corresponding reference circuit as Figure 5-5 and Figure 5-6:

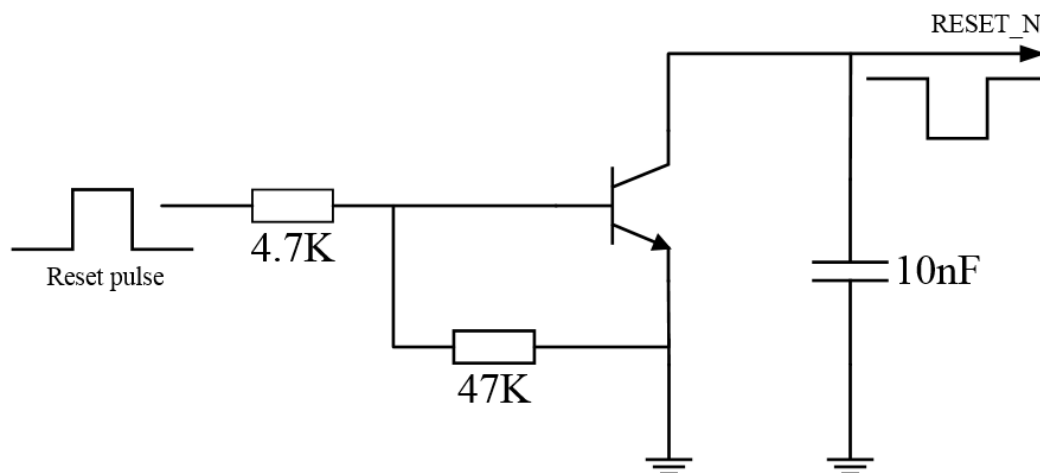


Figure 5-5 OC Driven Reset Reference Circuits

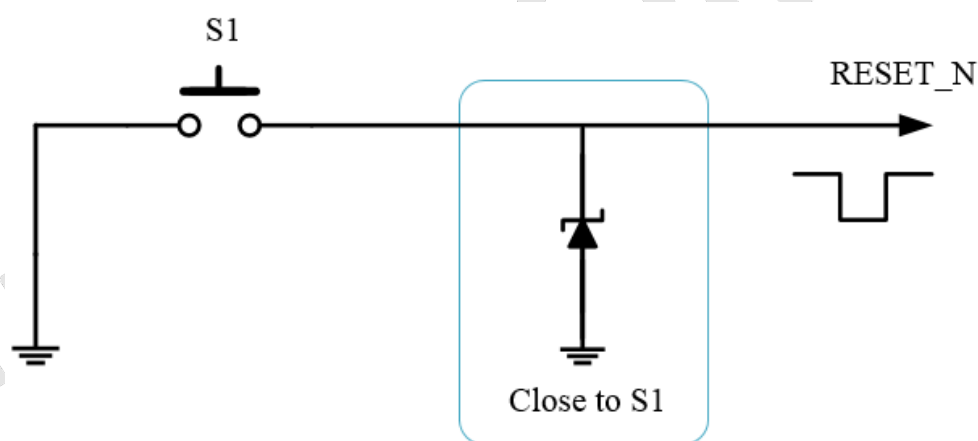


Figure 5-6 Button Reset Reference Circuits

The reset timing is shown as follows:

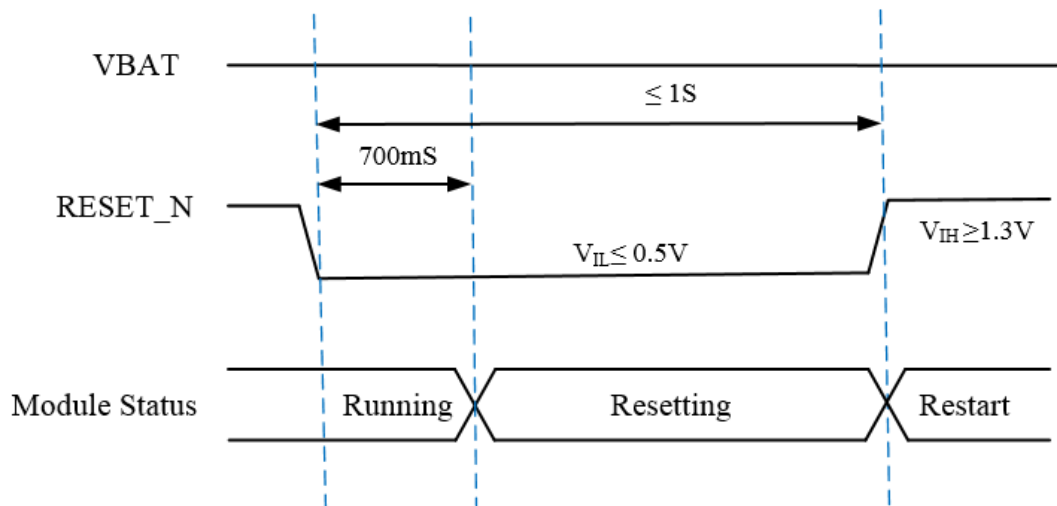


Figure 5-7 Reset Timing

## 5.2 Network status indicate interface

NL668-EU series module provides three network status indicate pins. Pin 5 is network status indicator by default, AT commands AT+LEDCFG can switch to pin6 or pin61, table 5-4 is the pin definition.

PIN Name	I/O	PIN Num.	Description
NET_MODE	O	5	Network status indicator (by default)
NET_STATUS	O	6	Network status indicator
STATUS	O	61	Network status indicator

Table 5-4 Network Status Indicate

### 5.2.1 Interface status description

Network status indicate pins are used to driven indicate light and describe module's network status, NL668-EU series module network indicate light work status description as follow table:

Mode	Module Network indicator pin status	Indicator light flash/off status	Description
1	600ms High/600ms Low	Flash 600ms on /600ms off	No SIM card Request SIM PIN Registering network ( $T < 15S$ ) Register network failed
2	3000ms High /75ms Low	Slow flash 3000ms on/75ms off	Standby
3	75ms High / 75ms Low	Speed flash	Data link established

Mode	Module Network indicator pin status	Indicator light flash/off status	Description
		75ms on/75ms off	
4	Low	Off	Voice call
5	High	on	Sleep

Table 5-5 Network Indicate Light Work Status

NL668-EU series module network indicate light reference design circuits shown as follows:

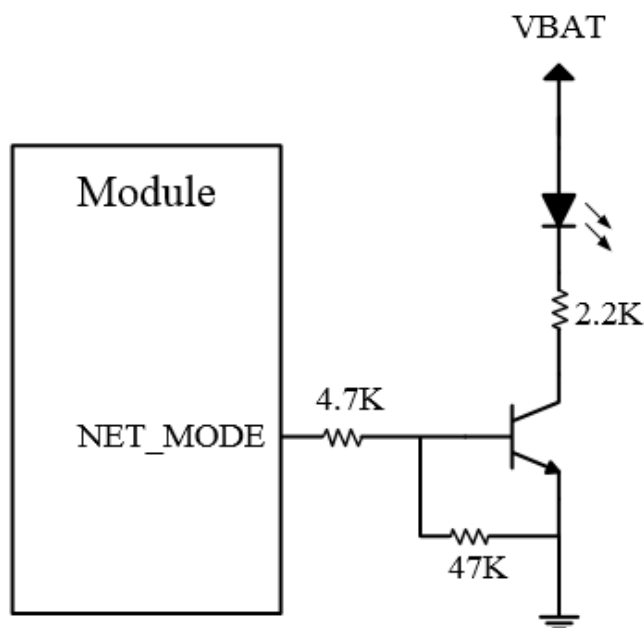


Table 5-6 Network Indicate Light Reference Circuits

## 5.3 (U)SIM card interface

NL668-EU series module has built-in (U)SIM card interface, and supports 1.8V and 3.0V (U)SIM card.

### 5.3.1 (U)SIM pin definition

(U)SIM pin definition is shown in the following table:

Pin name	I/O	Pin Num.	Description
USIM_PRESENCE	I	13	Detect (U)SIM card for Hot-swap
USIM_VDD	PO	14	(U)SIM Power
USIM_DATA	IO	15	(U)SIM DATA
USIM_CLK	O	16	Clock Signal
USIM_RESET	O	17	Reset Signal

Table 5-7 (U)SIM Card Pin



## 5.3.2 (U)SIM interface circuit

### 5.3.2.1 (U)SIM card connector with card detection signal

(U)SIM circuit design requires use (U)SIM card connector, recommend chose with card detect signal that support card hot swap function (Fibocom recommend: SIM016-8P-220P).

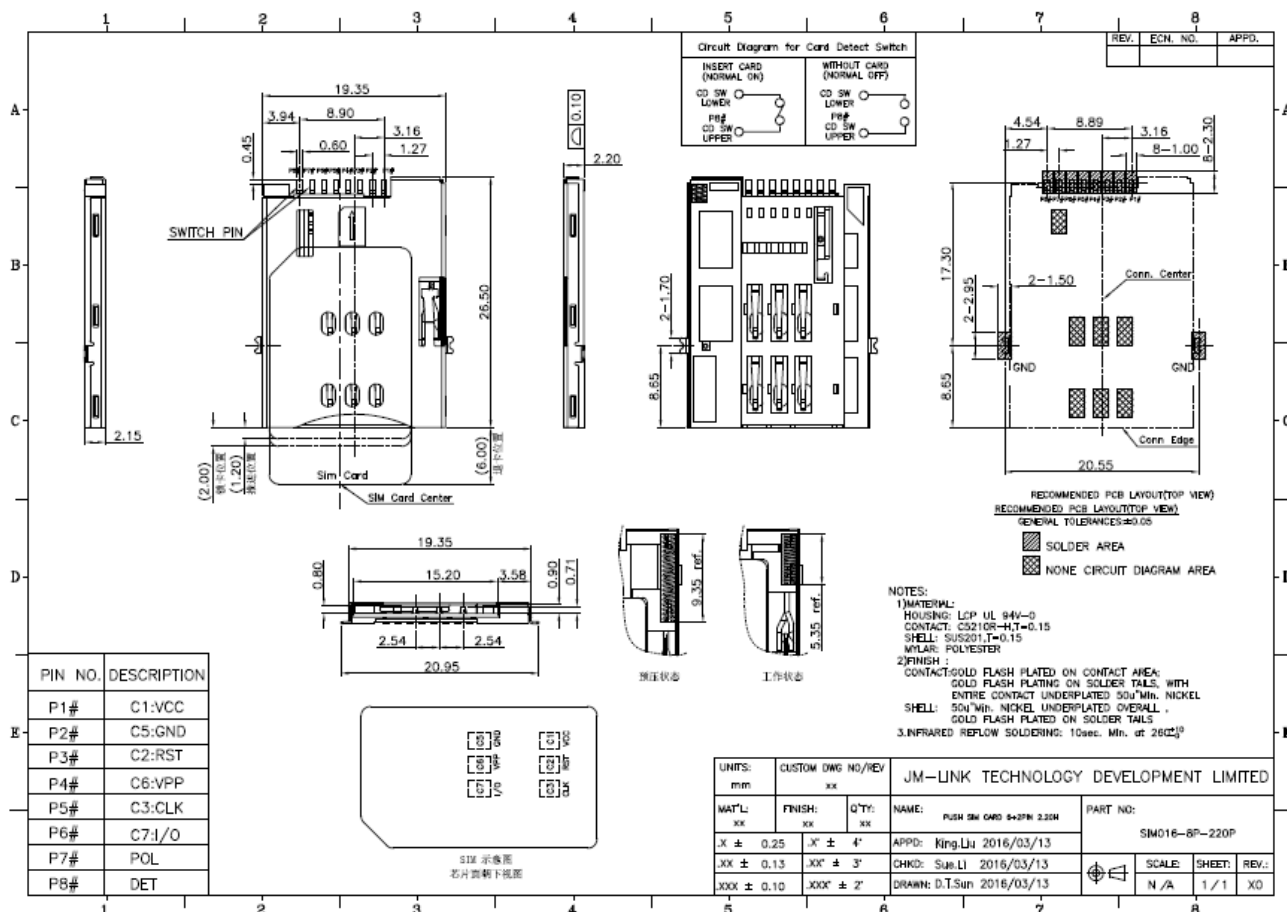


Figure 5-8 (U)SIM Card Connector (SIM016-8P-220P)

SIM016-8P-220P card socket, DET and POL are short connected when the card is inserted; DET and POL are disconnected when there is no card. The following is the reference design circuit, (U)SIM card insertion, USIM\_PRESENCE pin is high level; (U)SIM card plug out, USIM\_PRESENCE pin is low level.

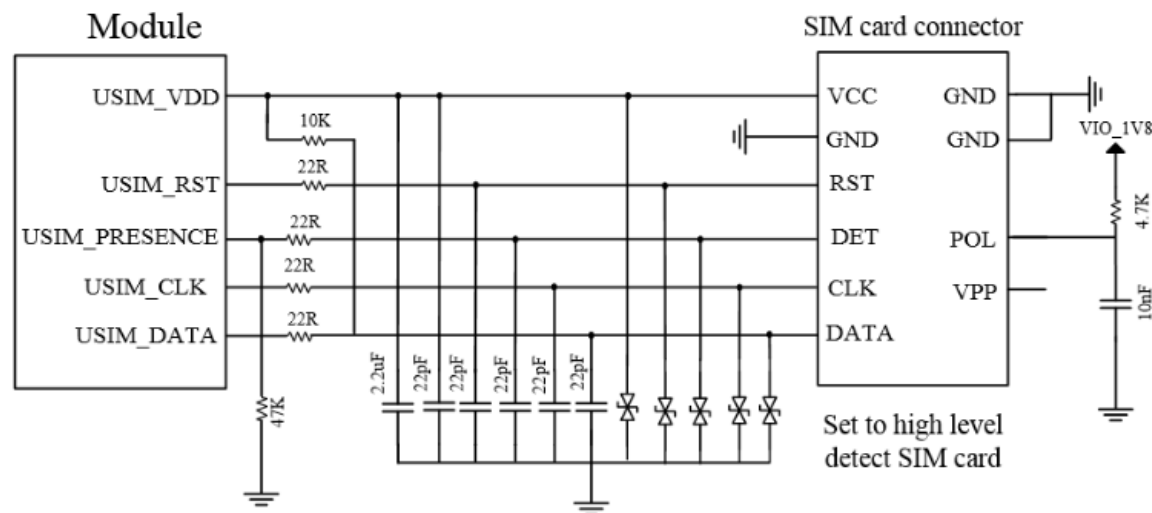


Figure 5-9 (U)SIM Card Connector with Detection Signal Reference Circuit

### 5.3.2.2 (U)SIM card connector without detection signal

If use (U)SIM card connector without detection signal USIM\_ PRESENCE pin must keep floating.

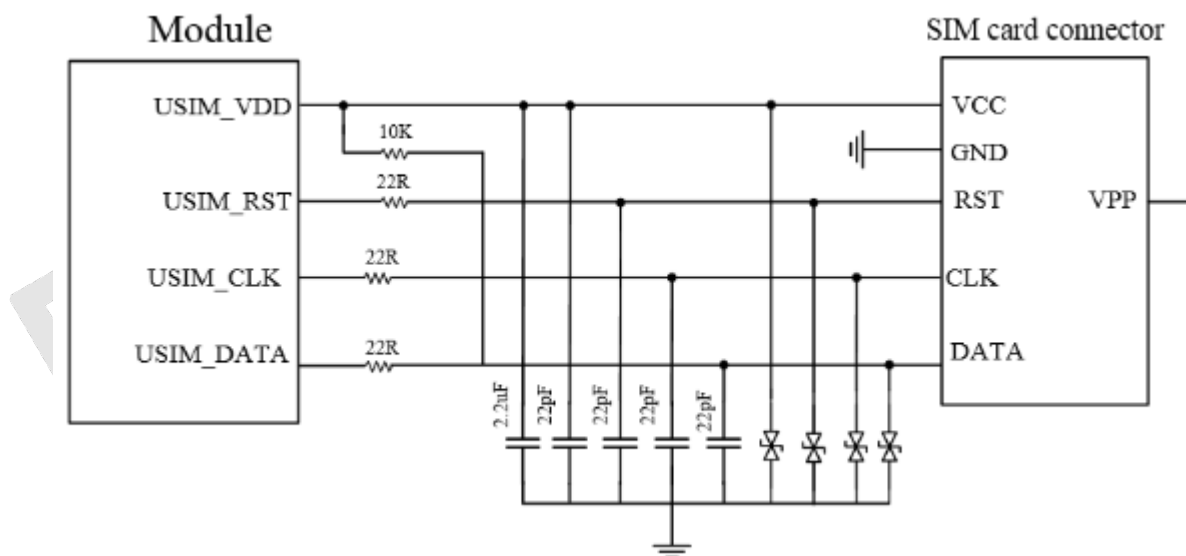


Figure 5-10 (U)SIM Card Connector without Detection Signal Reference Circuit

### 5.3.3 (U)SIM hot plug

NL668-EU series module determine the insertion and removal of (U)SIM card by detect the USIM\_ PRESENCE pin state and achieve hot plug function

The card hot plug function can be configured by the “AT+MSMPD” command, and the AT commands are shown in the following table:

AT command	(U)SIM card hot plug detection	Function description
AT+MSMPD=1	Enabled	Default, SIM card hot plug detection is enabled The module detects whether the SIM card is

AT command	(U)SIM card hot plug detection	Function description
		inserted through the USIM_PRESENCE pins' state
AT+MSMPD=0	Disabled	SIM card hot plug detection function is disabled The module read the (U)SIM card when module power on, and does not detect the USIM_PRESENCE state

Table 5-8 (U)SIM Card Hot Plug Function Configured

After enabled the hot plug detection function of the (U)SIM card, if USIM\_PRESENCE is in high level, the module will detect the (U)SIM card insertion and execute card initialization program. After reading the (U)SIM card information, the module will register network. When the USIM\_PRESENCE is in low level, the module detects (U)SIM card is removed, and it will not read the (U)SIM card.



**Note:**

The USIM\_PRESENCE pin active high by default, and can be switched to active low by AT command.

AT command	Function description
AT+GTSET=" SIMPHASE",1	Default, high level detects (U)SIM card
AT+GTSET=" SIMPHASE",0	Low level detects (U)SIM card

Table 5-9 USIM\_PRESENCE Effective Level Switched

### 5.3.4 (U)SIM design requirements

(U)SIM card circuit design shall meet EMC standards and ESD requirements, and at the same time, shall improve anti-interference ability to ensure that the (U)SIM card can work stably. The design needs to strictly observe the following rules:

- (U)SIM card connector is placed as close to the module as possible, away from the RF antenna, DCDC power, clock signal lines and other strong interference sources;
- Adopt the (U)SIM card connector with metal shield shell to improve anti-interference ability;
- The length of cable from the module to the (U)SIM card connector shall not exceed 100mm. Longer cable reduces signal quality.
- USIM\_CLK and USIM\_DATA signals are ground isolated to avoid mutual interference. If it is difficult to do so, (U)SIM signal needs to be ground protected as a set;
- The filter capacitor and ESD device of (U)SIM card signal cable should place close to the (U)SIM card connector.
- Please select equivalent capacitor is 22pF~33pF capacitor for ESD device.
- USIM\_DATA should pull up to USIM\_VDD with a 10K resistor.

## 5.4 USB interface

### 5.4.1 USB Pin definition

Pin name	I/O	Pin Num.	Description
USB_DP	IO	69	USB differential data bus D+
USB_DM	IO	70	USB differential data bus D-
USB_VBUS	PI	71	USB Plug detect

Table 5-10 USB Pin Definition

For more information about the USB 2.0 specification, please refer to <http://www.usb.org/home>



#### Note:

Since the module supports USB 2.0 High-Speed, TVS tube equivalent capacitance on the USB\_DM/DP differential signal cable is required to be less than 1pF, and a 0.5pF capacitance TVS is recommended. Connect a 0-ohm resistor to USB\_DM / DP differential line to help analyze problems.

USB\_DM and USB\_DP are high-speed differential signal cables, can achieve the maximum transmission rate of 480Mbps/s, and must follow the rules below in PCB Layout:

- USB\_DM and USB\_DP signal cable's control differential impedance is 90 ohm
- USB\_DM and USB\_DP signal cables shall be parallel and equal in length, and avoid the right-angle route;
- USB\_DM and USB\_DP signal cables are routed on the signal layer closest to the ground layer, and the cables shall be grounded;

## 5.5 UART Interface

### 5.5.1 UART interface definition

NL668-EU series module has two serial ports: the main serial port and debug serial port. The main serial ports support 4800bps, 9600bps, 19200bps, 38400bps, 57600bps, 115200bps, 230400bps baud rate.

The default baud rate is 115200bps, used for data transmission and AT command transmission.

Debug serial port support 115200bps baud rate for FIBOCOM internal debug. The following table are the pin definition of main serial port and debug port.

Pin name	I/O	Pin Num	Description
RI	O	62	Ring indicator
DCD	O	63	Data carrier detection
CTS	I	64	Clear to send. (apply to NL668-EU-00/01)

Pin name	I/O	Pin Num	Description
	O		Clear to send. (apply to NL668-EU-03)
RTS	O	65	Request to send(apply to NL668-EU-00/01)
	I		Request to send(apply to NL668-EU-03)
DTR	I	66	Sleep mode control
TXD	O	67	Module Transmit data
RXD	I	68	Module Receive data

Table 5-11 Main Serial Port

Pin name	I/O	Pin Num	Description
DBG_RXD	I	11	Module Receive data
DBG_TXD	O	12	Module Transmit data

Table 5-12 Debug Serial Port

## 5.5.2 UART port application

The serial port level of NL668-EU series module is 1.8V, if the level of the client host system is 3.3V or other, level translator needed between the module and the host. The reference design circuit of level translator is shown as follows:

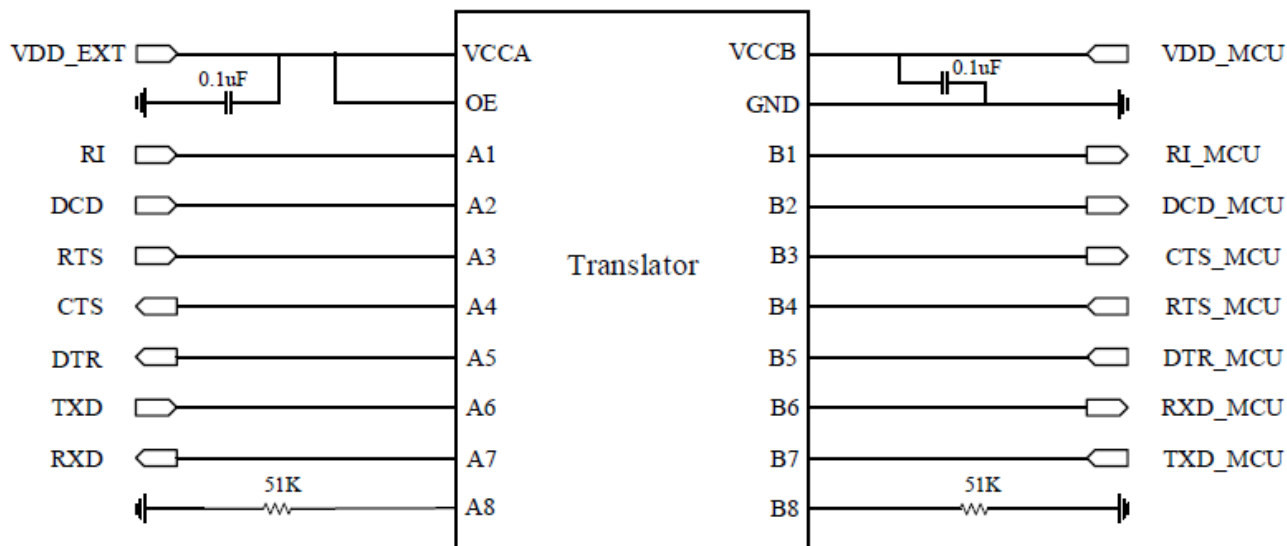


Figure 5-11 UART Level Translate Reference 1 (apply to NL668-EU-00/01)

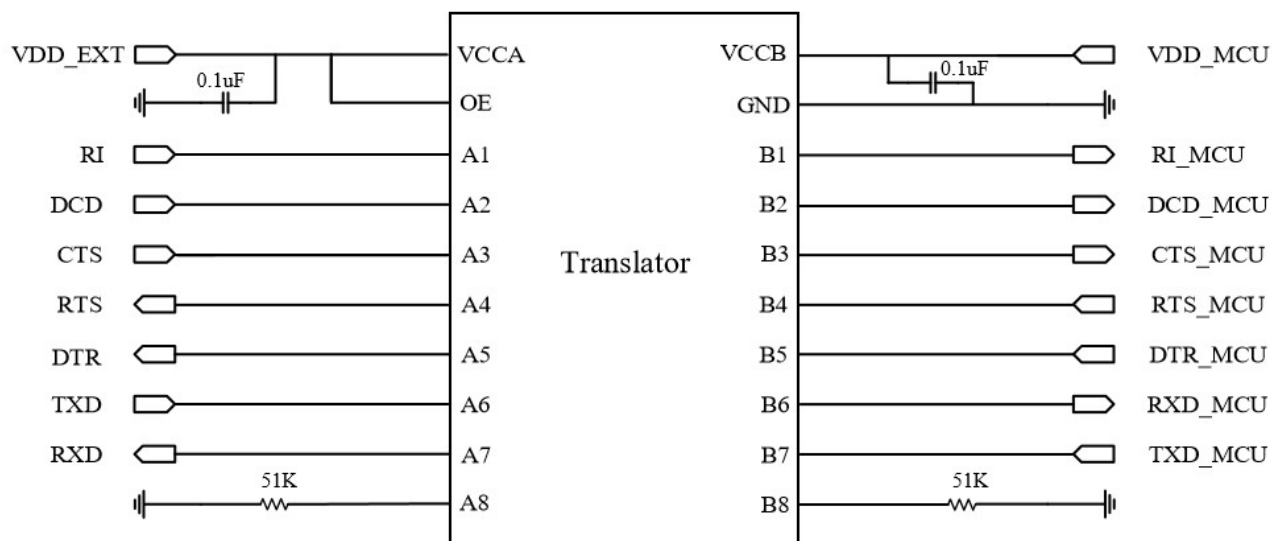


Figure 5-12 UART Level Translate Reference 2 (apply to NL668-EU-03)

The other level translator circuit is shown as Figure 5-12, The rest input and output circuit design of dotted line please refer to solid line part, but pay attention to signal connection direction.

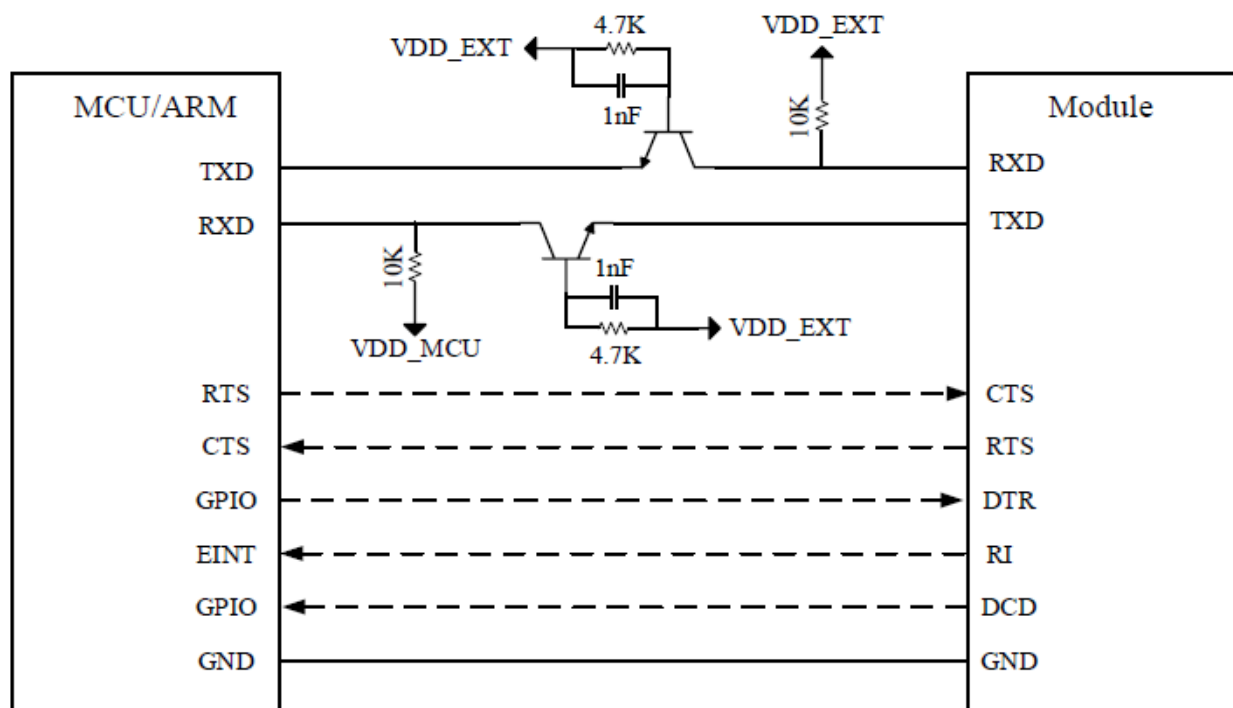


Figure 5-13 UART Level Translate Reference 3

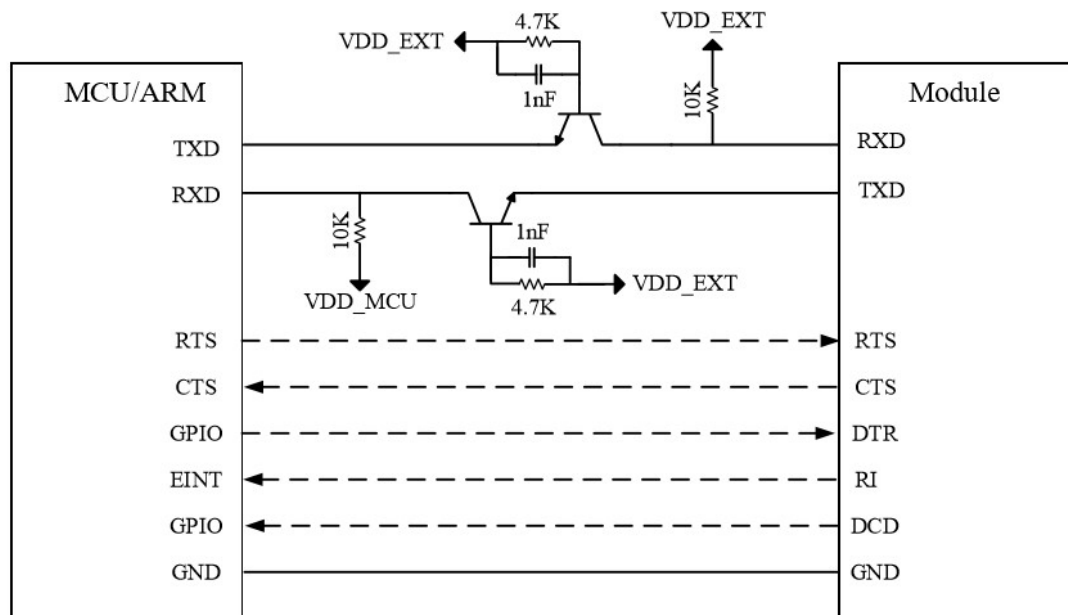


Figure 5-14 UART Level Translate Reference 4



**Note:**

Level translate circuits is not suitable for applications of baud rates above 460Kbps.

## 5.6 ADC interface

NL668-EU series module support two channels ADC interface. Use AT+TADC command can read the value of ADC interface. The voltage range of ADC interface is 0.3V~VBAT\_BB.

PIN Name	I/O	Pin Num	Description
ADC0	I	45	Analog to digital converter interface 0
ADC1	I	44	Analog to digital converter interface 1

Table 5-13 ADC Pin Definition

## 5.7 PCM interface

NL668-EU series module provides a PCM interface for communication with digital audio devices such as an external CODEC.

### 5.7.1 Support model

Product model	Description
NL668-EU-00	Support
NL668-EU-01	Support
NL668-EU-03	Support

Table 5-14 Support Model of PCM

## 5.7.2 PCM interface definition

Pin Name	I/O	Pin Num.	Description
PCM_IN	I	24	PCM data input
PCM_OUT	O	25	PCM data output
PCM_SYNC	IO	26	PCM data synchronous signal
PCM_CLK	IO	27	PCM clock

Table 5-15 PCM Pin Definition

## 5.7.3 PCM interface description

Pin Name	Frequency.	Duty Cycle	Coded Format	Operating Mode	Description
PCM_CLK	2.048MHz	50%	16bit Liner mono	Module serves as master that supports PCM	PCM CLK
PCM_OUT	-	-			PCM Output
PCM_IN	-	-			PCM Input
PCM_SYNC	8KHz	Short Pulse			PCM Synchronous Signal (Falling edge sampling)

Table 5-16 PCM Interface Description

NL668-EU series module adopts the above configuration by default, any adjustment, please contact Fibocom wireless technical support.

## 5.7.4 PCM signal description

The PCM signal of NL668-EU series module adopts domestic mainstream Europe E1 standard. PCM\_CLK frequency is 2.048MHz clock in 16bit linear format encoding. PCM\_SYNC is a 8kHz burst (488nS).

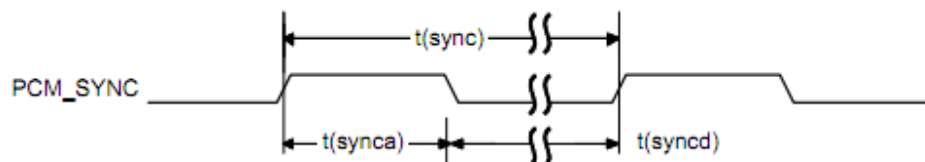


Figure 5-15 PCM\_SYNC Timing



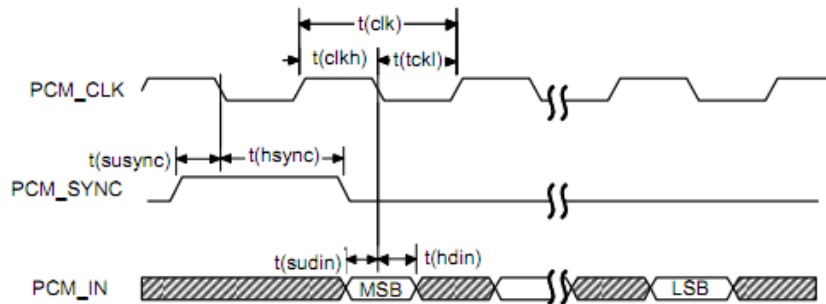


Figure 5-16 PCM\_CODEEC to NL668-EU Timing

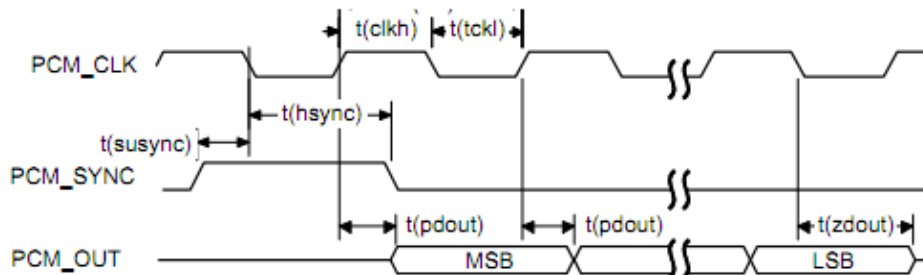


Figure 5-17 NL668-EU to PCM\_CODEEC Timing

Parameter		Min	Typ	Max	Unit
t(sync)	PCM_SYNC cycle time	–	125	–	μs
t(synca)	PCM_SYNC asserted time	–	488	–	ns
t(syncd)	PCM_SYNC deasserted time	–	124.5	–	μs
t(clk)	PCM_CLK cycle time	–	488	–	ns
t(clkh)	PCM_CLK high time	–	244	–	ns
t(tckl)	PCM_CLK low time	–	244	–	ns
t(susync)	PCM_SYNC offset time to PCM_CLK falling	–	122	–	ns
t(sudin)	PCM_DIN setup time to PCM_CLK falling	60	–	–	ns
t(hdin)	PCM_DIN hold time after PCM_CLK falling	10	–	–	ns
t(pdout)	Delay from PCM_CLK rising to PCM_DOUT valid	–	–	60	ns
t(zdout)	Delay from PCM_CLK falling to PCM_DOUT high impedance	–	160	–	ns

Table 5-17 Codec Timing Parameters

## 6 Low Power Consumption

### 6.1 Airplane mode

W\_DISABLE # Pin Description:

Pin name	I/O	Pin NO.	Description
W_DISABLE#	I	4	Module airplane mode control

Table 6-1 W\_DISABLE# Pin Description

NL668-EU series module supports two ways to enter airplane mode:

1	Hardware I/O interface button control	First send "AT+WDISABLEEN=1" to enable W_DISABLE# pin function. Pull high or float W_DISABLE# pin (pull high by default), module enter normal mode, pull it down, module enter airplane mode.
2	AT command control	AT+CFUN=4--module enter airplane mode AT+CFUN=1--module enter normal mode

Table 6-2 Module Enter Airplane Mode Ways

### 6.2 Sleep mode

#### 6.2.1 USB Application (nonsupport USB suspend, support VBUS)

If the host nonsupport USB suspend function, the module can enter sleep mode by disconnect USB\_VBUS from the external control circuit:

##### Sleep:

Send AT+GTLPMODE=1,X command to set the WAKEUP\_IN pin's level of control module enter sleep mode. Reset module, command effective.

(X=0, WAKEUP\_IN pin is high level, module enter sleep mode;

X=1, WAKEUP\_IN pin is low level, module enter sleep mode)

AT+CSCLK=1 command to enable sleep function.

AT+GTUSBSLEEPEN=1,0 command to set USB sleep mode.

Draw out the USB cable or disable the USB HUB controller, module enter sleep mode.

##### Wake up:

Plug in USB cable or enable the USB HUB controller can wake up the module.

#### 6.2.2 USB application (nonsupport USB suspend, nonsupport VBUS)

If the host nonsupport USB suspend and nonsupport VBUS function, the module can enter sleep mode

by disconnect USB\_VBUS from the external control circuit:

**Sleep:**

Send AT+GTLPMODE=1,X command to set the WAKEUP\_IN pin's level of control module enter sleep mode. Reset module, command effective.

(X=0, WAKEUP\_IN pin is high level, module enter sleep mode;

X=1, WAKEUP\_IN pin is low level, module enter sleep mode)

AT+CSCLK=1 command to enable sleep function.

AT+GTUSBDETECTEN=1 command to enable the USB software detection function

AT+GTUSBSLEEPEN=1,0 command to set USB sleep mode

Draw out the USB cable or disable the USB HUB controller, module enter sleep mode.

**Wake up:**

Plug in USB cable or enable the USB HUB controller can wake up the module.

### 6.2.3 USB application (Supports USB Suspend)

If the host support USB Suspend/Resume. Setting USB sleep in Linux system.

**Sleep:**

Send AT+GTLPMODE=1,X command to set the WAKEUP\_IN pin's level of control module enter sleep mode. Reset module, command effective.

(X=0, WAKEUP\_IN pin is high level, module enter sleep mode;

X=1, WAKEUP\_IN pin is low level, module enter sleep mode)

AT+CSCLK=1 command to enable sleep function.

AT+GTUSBSLEEPEN=0,0 command to set USB sleep mode

In Linux system, set the level and control of USB device as auto to suspend the devices of module.

Standing the module and host about 2 seconds, the module can enter suspend mode automatically.

**Wake up:**

Any operation on USB can wake up the module from sleep mode.

### 6.2.4 UART application ( WAKEUP\_IN pin level control )

When host and module connected through UART, use the following steps to make the module enter sleep mode:

Sent AT+GTLPMODE=1,X command to set et the WAKEUP\_IN pin's level of control module enter sleep mode. Reset module, command effective.

(X=0, WAKEUP\_IN pin is high level, module enter sleep mode;

X=1, WAKEUP\_IN pin is low level, module enter sleep mode)

AT+CSCLK=1 command to enable sleep function.

AT+GTUSBSLEEPEN=2,X command to disable USB function (X can be 0 or 1)

#### Wake up:

The level of WAKEUP\_IN pin contrary with that when the module enter sleep mode can wake up module.

(X=0, WAKEUP\_IN pin is low level, wake up module;

X=1, WAKEUP\_IN pin is high level, wake up module)

### 6.2.5 UART application ( DTR pin level control )

When host and module connected through UART, use the following steps can make the module enter

#### Sleep mode:

Send AT+GTLPMODE=2,X command to set the DTR set pin's level of control module enter sleep mode. Reset module, command effective.

(X=0, DTR pin is high level, module enter sleep mode;

X=1, DTR pin is low level, module enter sleep mode)

AT+CSCLK = 1 command to enable sleep function.

AT+GTUSBSLEEPEN=2,X command to disable USB function (X can be 0 or 1)

The level of DTR pin contrary with that when the module enter sleep mode can wake up module. (X=0, DTR pin is low level, wake up module; X=1, DTR pin is high level, wake up module)

### 6.2.6 ATS24 Command

ATS24 command can also make module enter sleep mode.

#### Sleep:

Send AT+GTLPMODE=0 Reset module, command effective.

ATS24=X command to into sleep after X seconds. (X is nonzero integer)

AT+GTUSBSLEEPEN=2,X command to disable USB function (X can be 0 or 1)

#### Wake up:

Wake up the module by send the AT command fast. If don't send AT commands between X seconds, module will try to enter sleep mode.



#### Note:

Since the level of UART sleep power is different, power consumption of use ATS24 command to enter sleep mode is higher than that use Pin control to enter sleep mode.

When ATS24 command enter sleep mode countdown, it isn't enter sleep mode once overtime strictly, but try to enter sleep mode. If system don't support after overtime, it will timekeeping automatically.

If you want to use the RI signal to represent the state of the module, please refer to the AT+GTWAKE command in FIBOCOM AT Commands User Manual\_Sleep.

For more sleep command description, please refer to 《FIBOCOM AT Commands User Manual\_Sleep》

## 7 RF interface

NL668-EU series module has ANT\_MAIN, ANT\_DIV and ANT\_ GNSS three antenna interfaces, its pin definition show as table 7-1:

Pin Name	I/O	Pin Num.	Description
ANT_DIV	I	35	Diversity antenna
ANT_GNSS	I	47	GPS antenna
ANT_MAIN	IO	49	Main antenna

Table 7-1 RF Interface

### 7.1 Operating band

Operating Band	Description	Mode	Tx (MHz)	Rx (MHz)
Band 1	IMT 2100MHz	LTE FDD/WCDMA	1920 - 1980	2110 - 2170
Band 3	DCS 1800MHz	LTE FDD/GSM	1710 - 1785	1805 - 1880
Band 5	CLR 850MHz	LTE FDD/WCDMA/GSM	824 - 849	869 - 894
Band 7	IMT-E 2600Mhz	LTE FDD	2500 - 2570	2620 - 2690
Band 8	E-GSM 900MHz	LTE FDD/WCDMA/GSM	880 - 915	925 - 960
Band 20	EUDD 800MHz	LTE FDD	832 - 862	791 - 821
Band 38	IMT-E 2600MHz	LTE TDD	2570 - 2620	
Band 40	IMT 2300MHz	LTE TDD	2300 - 2400	
Band 41	BRS/EBS 2500MHZ	LTE TDD	2555~2655	

Table 7-2 Operating Band

### 7.2 Transmission Power

The Transmission Power of NL668-EU series module show as follows:

Mode	Band	Tx Power(dBm)	Note
GSM	GSM 850	32.5+1/-1.5	
	GSM 900	32.5+1/-1.5	
	DCS 1800	29.5+1/-1.5	
WCDMA	Band I	23.5+1/-1.5	
	Band V	23.5+1/-1.5	

Mode	Band	Tx Power(dBm)	Note
	Band VIII	23.5+1/-1.5	
LTE FDD	Band 1	23+1/-1.5	10MHz Bandwidth, 1 RB
	Band 3	23+1/-1.5	10MHz Bandwidth, 1 RB
	Band 5	23+1/-1.5	10MHz Bandwidth, 1 RB
	Band 7	23+1/-1.5	10MHz Bandwidth, 1 RB
	Band 8	23+1/-1.5	10MHz Bandwidth, 1 RB
	Band 20	23+1/-1.5	10MHz Bandwidth, 1 RB
LTE TDD	Band 38	23+1/-1.5	10MHz Bandwidth, 1 RB
	Band 40	23+1/-1.5	10MHz Bandwidth, 1 RB
	Band 41	23+1/-1.5	10MHz Bandwidth, 1 RB

Table 7-3 Output Power

## 7.3 Receive Sensitivity

Mode	Band	Rx Sensitivity(dBm) PRX Typical	Rx Sensitivity(dBm) DRX Typical	Note
GSM	GSM 850	-109	-	BER<2.43%
	GSM 900	-109.5	-	BER<2.43%
	DCS 1800	-109	-	BER<2.43%
WCDMA	Band I	-111	-	BER<0.1%
	Band V	-111	-	BER<0.1%
	Band VIII	-111	-	BER<0.1%
LTE FDD	Band 1	-98.5	-99	10MHz Band width
	Band 3	-99	-99	10MHz Band width
	Band 5	-99.5	-99.5	10MHz Band width
	Band 7	-97	-97.5	10MHz Band width
	Band 8	-99	-99	10MHz Band width
	Band 20	-98.5	-99.5	10MHz Band width
LTE TDD	Band 38	-98	-96.5	10MHz Band width
	Band 40	-98	-97	10MHz Band width
	Band 41	-98	-96	10MHz Band width

Table 7-4 Receive Sensitivity



**Note:**

The sensitivity of above table is the result of main and diversity test separately, if tested with PRX and DRX together, the result will rise about 3dB.

## 7.4 GNSS Receiver

### 7.4.1 GNSS specification

The NL668-EU module supports the GPS/GLONASS/BeiDou functions using Qualcomm Gen8 technology. Its specification show as follows:

Description		Condition	Typ.
Current consumption ( AT+CFUN=0 )		GNSS fixing	62mA
		GNSS tracking	62mA
		Standby	33mA
TTFF	GNSS	Cold start	45s
		Warm start	40s
		Hot Start	5s
Sensitivity		fixing	-145dbm
		tracking	-156dbm
	CN0	GNSS Signal@-130dBm	38.5dB-HZ
Positional Accuracy	CEP	GNSS Signal @-130dBm	<3m

Table 7-5 GNSS Specification



**Note:**

The current in above table test with USB plug in.

### 7.4.2 GNSS observes protocol

NL668-EU series module adopt NMEA-0183 protocol.

## 7.5 Antenna design

### 7.5.1 Antenna index

#### 1) Antenna efficiency

Antenna efficiency is the ratio of antenna input power to radiated power. Due to the antenna return loss, material loss, and coupling loss, the radiated power is always lower than the input power. Recommend> 40% (-4dB).

## 2) S11 or VSWR

S11 shows that the matching degree of the antenna's 50 ohm impedance, to a certain extent, affects the antenna efficiency. VSWR test methods can be used to measure this parameter. Recommend S11 <-10dB.

## 3) Polarization

Polarization is the rotation direction of the electric field in the maximum radiation direction of the antenna. It is recommended to use linear polarization.

## 4) Radiation pattern

Radiation pattern refers to the antenna's electromagnetic field strength in the far field in all directions. Half-wave dipole antenna is the most suitable terminal antenna. For built-in antenna, PIFA antennas or IFA antennas are recommended:

Antenna area: 6mm high\*10mm wide\*100mm long.

Antenna radiation direction: Omni\_directional(all direction).

## 5) Gain and directivity

Antenna directivity refers to the electromagnetic field strength of electromagnetic wave in all directions. Gain is a collection of antenna benefits and antenna directivity.

Recommended antenna gain ≤2.5dBi.

## 6) Interference

In addition to the antenna performance, other interferences on the PCB also affect the performance of the module. In order to ensure the high performance of the module, interference must be controlled. Suggestions: For example, LCD, CPU, FPC cable, audio circuit, power supply should be away from the antenna as far as possible, and make the appropriate isolation and shielding, or filtering on the path.

## 7) Antenna index requirements

NL668-EU module main antenna requirements	
Frequency range	It must use the most suitable antenna to adapt to the relevant frequency band
Bandwidth (GSM/EDGE)	GSM900: 80 MHz GSM850: 70 MHz GSM1800(DCS): 170 MHz
Bandwidth (WCDMA)	WCDMA band I (2100): 250 MHz WCDMA band V (850): 70 MHz WCDMA band VIII (900): 80 MHz
Bandwidth (LTE)	LTE band 1(2100): 250 MHz LTE Band 3(1800): 170 MHz LTE Band 5(850): 70 MHz



NL668-EU module main antenna requirements	
	LTE Band 7(2600): 190 MHz LTE Band 8(900):80 MHz LTE Band 20(800): 71 MHz LTE band 38(2600): 50 MHz LTE band 40(2300): 100 MHz LTE band 41(2500): 100 MHz
Impedance	50 ohms
Input power	> 33dBm(2W) peak power GSM > 23.5dBm average power WCDMA & LTE
Standing wave ratio recommended	≤ 2:1

Table 7-6 Main Antenna Requirements

## 7.5.2 Antenna reference design

Antenna is a sensitive device, susceptible to the external environment. For example, the size of the module, the location of the antenna, the space it occupies, and the surrounding ground all may affect antenna performance. In addition, the RF cable connect with antenna, and the location of the fixed antenna also may affect its performance. NL668-EU series module's three antenna all led by welding plate. recommended clients use the U.FL-R-SMT-1 antenna connector and corresponding match adapter cable. Figure 7-1 is reference design of main antenna and diversity antenna.

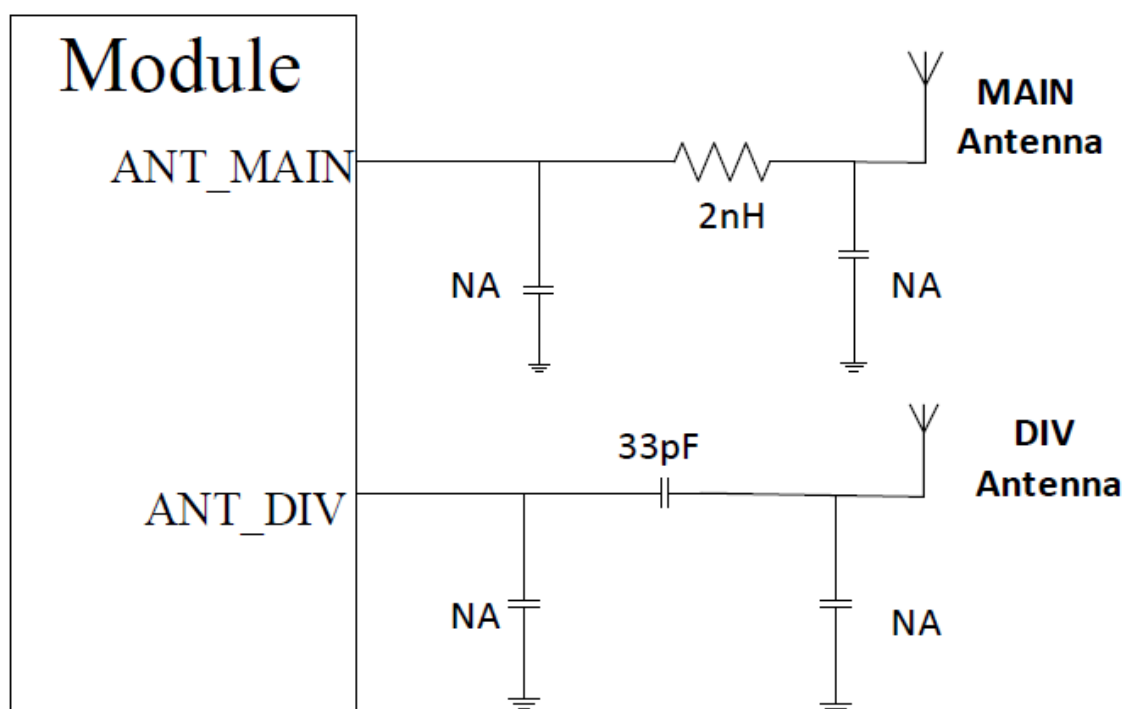


Figure 7-1 Main and diversity Antenna Reference Circuit

Figure 7-2 is reference design of GNSS antenna.

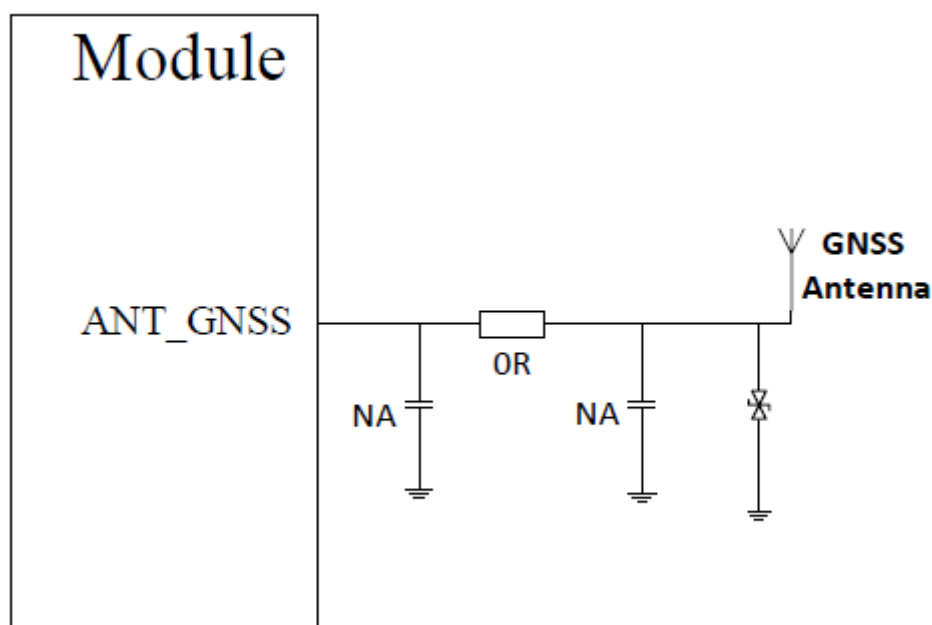


Figure 7-2 GNSS Antenna Reference Circuit



**Note :**

- All matches must be placed close to antenna to make sure the characteristic impedance of

transmission cable is 50 ohms.

- Since the antenna loss should be less than 0.3dB, keep PCB cable as short as possible.
- Keep the PCB LAYOUT straight, and reduce holes on the route to another layer; also avoid right-angle and acute-angle wiring.
- PCB cable should have a good reference ground to avoid other signal cable near the antenna.
- Recommend a complete ground level, and use this complete ground level as a reference ground.
- Ground around antenna must be keep connect with main ground.
- For more design information please refer to 《FIBOCOM RF Antenna Application Design Instruction》

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## 8 Reliability

### 8.1 Limiting voltage range

The limiting voltage range is maximum voltage range that power supply and digital or analog input/output interfaces can withstand.

#### 8.1.1 Absolute voltage range

The absolute voltage range of NL668-EU series module is shown as table 8-1.

Parameter	description	Min	Typ	Max	Unit
VBAT	Power supply	-0.3	3.8	4.7	V
GPIO	Digital IO supply voltage	-0.3	1.8	2.0	V

Table 8-1 Absolute Voltage Range

#### 8.1.2 Operating voltage range

$V_L$  : logic low level ;  $V_H$  : logic high level ;

Parameter	$V_L$		$V_H$		Unit
	Min	Max	Min	Max	
Digital input	-0.3	0.6	1.2	2.0	V
Digital output	-	0.45	1.35	-	V

Parameter	I/O	Min	Typ	Max	Unit
VBAT	I	3.3	3.8	4.3	V
USIM_VDD	O	1.7/2.75	1.8/2.85	1.9/2.95	V

Table 8-2 Operating Voltage Range

### 8.2 Environment temperature range

The recommended operating temperature range of NL668-EU series module is  $-30^{\circ}\text{C} \sim +75^{\circ}\text{C}$ . When module operating at limited temperature range, some RF indexes may exceed standard, so module application terminal should consider temperature control measurement. The module application terminal is recommended storage in certain temperature conditions. Modules out of the temperature range may not operate or may be damaged.

Temperature	Min	Typ	Max	Unit
Operating temperature	-30	25	75	$^{\circ}\text{C}$

Temperature	Min	Typ	Max	Unit
Limited operating temperature	-40		85	°C
Storage temperature	-40		85	°C

Table 8-3 Environment Temperature Range

## 8.3 Environmental reliability requirements

Test items	Test conditions						
Low temperature storage test	Temperature $-40^{\circ}\text{C}\pm 3^{\circ}\text{C}$ , 24 hours in shutdown state						
High temperature storage test	Temperature $+85^{\circ}\text{C}\pm 3^{\circ}\text{C}$ , 24 hours in shutdown state						
Temperature shock test	In shutdown state, 0.5 hour at $-40^{\circ}\text{C}$ and $+85^{\circ}\text{C}$ environment respectively, the temperature conversion time $< 3\text{min}$ , for 24 cycles						
High temperature and humidity test	Temperature $+85^{\circ}\text{C}\pm 3^{\circ}\text{C}$ , humidity 90 ~ 95% RH, 24 hours in shutdown state						
Low temperature operating test	Temperature $-30^{\circ}\text{C}\pm 3^{\circ}\text{C}$ , 24 hours in operating state						
High temperature operating test	Temperature $+75^{\circ}\text{C}\pm 3^{\circ}\text{C}$ , 24 hours in operating state						
Vibration test	Conduct vibration test according to the requirements shown in the table below: <table border="1"> <tr> <th>Frequency</th><th>Random vibration ASD (Acceleration Spectral Density)</th></tr> <tr> <td>5~20Hz</td><td><math>0.96\text{m}^2/\text{s}^3</math></td></tr> <tr> <td>20~500Hz</td><td><math>0.96\text{m}^2/\text{s}^3(20\text{Hz})</math>, other <math>-3\text{dB/octave}</math></td></tr> </table>	Frequency	Random vibration ASD (Acceleration Spectral Density)	5~20Hz	$0.96\text{m}^2/\text{s}^3$	20~500Hz	$0.96\text{m}^2/\text{s}^3(20\text{Hz})$ , other $-3\text{dB/octave}$
Frequency	Random vibration ASD (Acceleration Spectral Density)						
5~20Hz	$0.96\text{m}^2/\text{s}^3$						
20~500Hz	$0.96\text{m}^2/\text{s}^3(20\text{Hz})$ , other $-3\text{dB/octave}$						
Connector life test	30 times of insertion/removal for RF antenna interface cable						

Table 8-4 Environmental Reliability Requirements

## 8.4 ESD characteristics

NL668-EU series module design has considered ESD issue and provided ESD protect measurements, but take ESD issue taken by module carrier and secondary development into consideration, developers should care ESD protection of module application terminal. In addition to considering anti-static treatment of packaging, please refer to recommended circuit of interface design in the document.

ESD allowable discharge range of NL668-EU series module show as table 8-5

Interface	Air discharge	Contact discharge
VBAT, GND	$\pm 10\text{KV}$	$\pm 5\text{KV}$
Antenna port	$\pm 8\text{KV}$	$\pm 4\text{KV}$

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Interface	Air discharge	Contact discharge
Other port	±1KV	±0.5KV

Table 8-5 ESD Allowable Discharge Rang

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## 9 Structure specification

### 9.1 Product appearance

The product appearance of NL668-EU series module is shown in Figure 9-1:

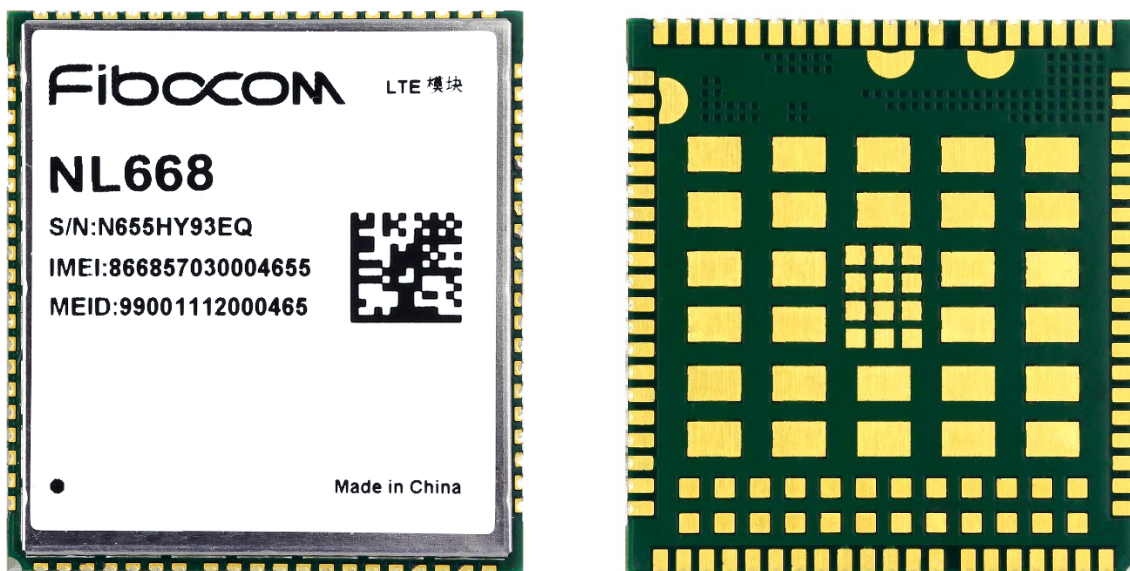


Figure 9-1 Product Appearance

### 9.2 Structure dimension

The structure dimension of NL668-EU series module is shown as Figure 9-2:

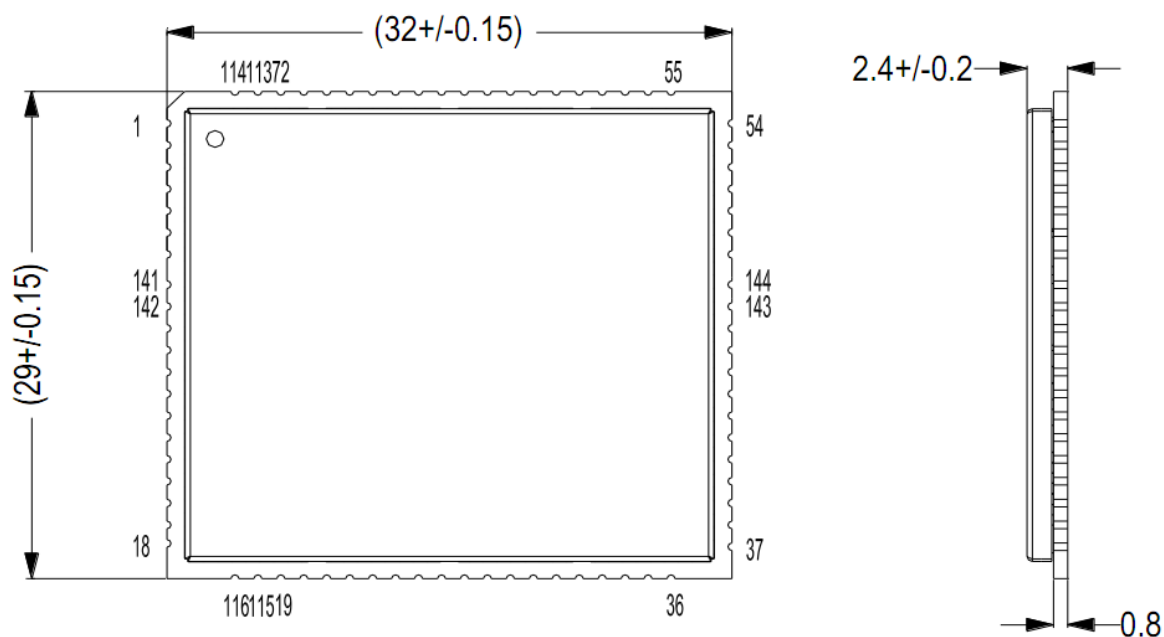


Figure 9-2 Structure Dimension (Unit: mm)

## 9.3 PCB Soldering Pad and Stencil Design

PCB soldering pad and stencil design please refer to 《FIBOCOM NL668 LCC SMT Design Description》.

## 9.4 SMT

SMT production process parameters and related requirements please refer to 《FIBOCOM NL668 LCC SMT Design Description》.

## 9.5 Carrier and storage

Carrier and storage please refer to 《FIBOCOM NL668 LCC SMT Design Description》.

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## 10 Approval

NL668-EU series module approval show as table 10-1:

Certification Scheme	NL668-EU-00		
CCC: Certificate for China Compulsory Product Certification)	✓	✓	
RED: Radio Equipment Directive	✓	✓	
NAL	✓	✓	
Radio Transmission Equipment Type Approval Certificate)	✓	✓	
RoHS	✓	✓	

Table 10-1 Approval

For more information please refer to Fibocom net.

# 11 Appendix

## 11.1 GPRS and EGPRS Encoding Scheme

Encoding method	CS-1	CS-2	CS-3	CS-4
Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data rate Kb/s	9.05	13.4	15.6	21.4

Table 11-1 GPRS Encoding Scheme

In the GPRS standard, 29 types of GPRS multislot modes are defined for use by mobile stations. The multislot class defines the maximum rate of uplink and downlink. The expression is 3+1 or 2+2, the first number indicates the number of downlink timeslots, and the second number indicates the number of uplink timeslots. Active timeslots indicate the total number of timeslots that the GPRS device can use for both uplink and downlink communications.

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4

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Multislot Class	Downlink Slots	Uplink Slots	Active Slots
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
33	5	4	6

Table 11-2 Multilevel Multislot Allocation

Coding Scheme	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
CS-1	GMSK	/	9.05kbps	18.1kbps	36.2kbps
CS-2	GMSK	/	13.4kbps	26.8kbps	53.6kbps
CS-3	GMSK	/	15.6kbps	31.2kbps	62.4kbps
CS-4	GMSK	/	21.4kbps	42.8kbps	85.6kbps
MCS-1	GMSK	C	8.80kbps	17.6kbps	35.2kbps
MCS-2	GMSK	B	11.2kbps	22.4kbps	44.8kbps
MCS-3	GMSK	A	14.8kbps	29.6kbps	59.2kbps
MCS-4	GMSK	C	17.6kbps	35.2kbps	70.4kbps
MCS-5	8-PSK	B	22.4kbps	44.8kbps	89.6kbps
MCS-6	8-PSK	A	29.6kbps	59.2kbps	118.4kbps
MCS-7	8-PSK	B	44.8kbps	89.6kbps	179.2kbps
MCS-8	8-PSK	A	54.4kbps	108.8kbps	217.6kbps
MCS-9	8-PSK	A	59.2kbps	118.4kbps	236.8kbps

Table 11-3 EGPRS Modulation and Encoding Method

## 11.2 Terms and acronyms

Term	Definition
AMR	Adaptive Multi-rate
bps	Bits Per Second
CS	Coding Scheme
DRX	Discontinuous Reception
EGSM	Extended GSM900 Band
FDD	Frequency Division Duplexing
GMSK	Gaussian Minimum Shift Keying
GSM	Global System for Mobile Communications
HSDPA	High Speed Down Link Packet Access
IMEI	International Mobile Equipment Identity
I <sub>max</sub>	Maximum Load Current
LED	Light Emitting Diode
LSB	Least Significant Bit
LTE	Long Term Evolution
CA	Carrier Aggregation
DLCA	Downlink Carrier Aggregation
SCell	Secondary Cell for CA
ME	Mobile Equipment
MS	Mobile Station
MT	Mobile Terminated
PCB	Printed Circuit Board
PDU	Protocol Data Unit

Term	Definition
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
RMS	Root Mean Square
RTC	Real Time Clock
Rx	Receive
SMS	Short Message Service
TDMA	Time Division Multiple Access
TE	Terminal Equipment
TX	Transmitting Direction
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver & Transmitter
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
USSD	Unstructured Supplementary Service Data
V <sub>max</sub>	Maximum Voltage Value
V <sub>norm</sub>	Normal Voltage Value
V <sub>min</sub>	Minimum Voltage Value
V <sub>IHmax</sub>	Maximum Input High Level Voltage Value
V <sub>IHmin</sub>	Minimum Input High Level Voltage Value

Term	Definition
VILmax	Maximum Input Low Level Voltage Value
VILmin	Minimum Input Low Level Voltage Value
VImax	Absolute Maximum Input Voltage Value
VImin	Absolute Minimum Input Voltage Value
VOHmax	Maximum Output High Level Voltage Value
VOHmin	Minimum Output High Level Voltage Value
VOLmax	Maximum Output Low Level Voltage Value
VOLmin	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access

Table 11-4 Terms and Acronyms

## 11.3 Related Document

- FIBOCOM EVK-GT8230-NL User Manual
- FIBOCOM ADP-NL668 Evaluation board instructions
- FIBOCOM NL668 LCC SMT Application Design Instruction
- FIBOCOM RF Antenna Application Design Instruction
- FIBOCOM NL668 AT Command Manual

## 11.4 Reference Standards

The design of the product complies with the following standards:

- 3GPP TS 51.010-1 V10.5.0: Mobile Station (MS) conformance specification; Part 1: Conformance specification
- 3GPP TS 34.121-1 V10.8.0: User Equipment (UE) conformance specification; Radio transmission and reception (FDD); Part 1: Conformance specification
- 3GPP TS 34.122 V10.1.0: Technical Specification Group Radio Access Network; Radio transmission and reception (TDD)
- 3GPP TS 36.521-1 V10.6.0: User Equipment (UE) conformance specification; Radio transmission

and reception; Part 1: Conformance testing

- 3GPP TS 21.111 V10.0.0: USIM and IC card requirements
- 3GPP TS 51.011 V4.15.0: Specification of the Subscriber Identity Module -Mobile Equipment (SIM-ME) interface
- 3GPP TS 31.102 V10.11.0: Characteristics of the Universal Subscriber Identity Module (USIM) application
- 3GPP TS 31.11 V10.16.0: Universal Subscriber Identity Module (USIM) Application Toolkit(USAT)
- 3GPP TS 36.124 V10.3.0: Electro Magnetic Compatibility (EMC) requirements for mobile terminals and ancillary equipment
- 3GPP TS 27.007 V10.0.8: AT command set for User Equipment (UE)
- 3GPP TS 27.005 V10.0.1: Use of Data Terminal Equipment - Data Circuit terminating Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)

## 11.5 Contact

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